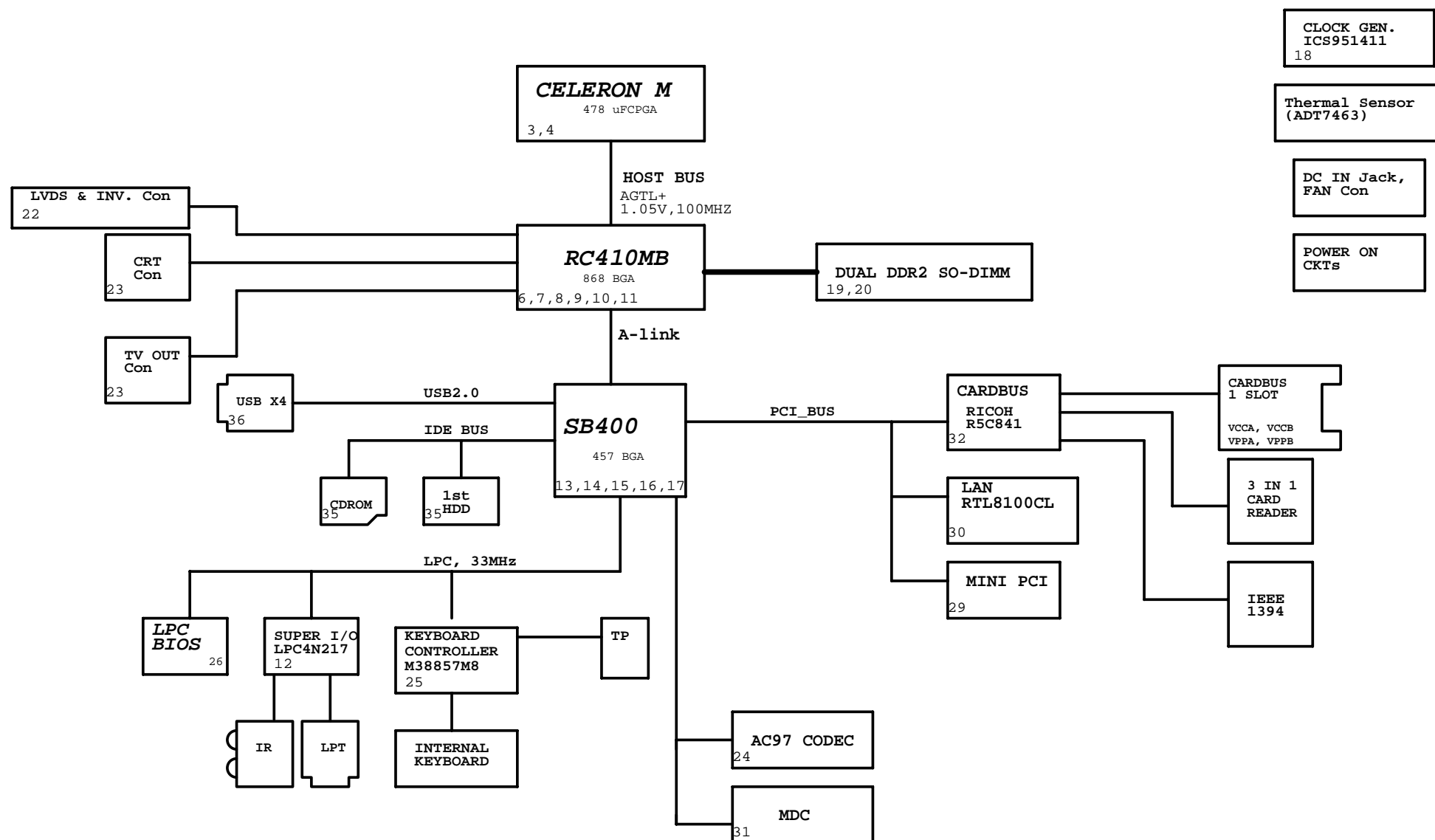
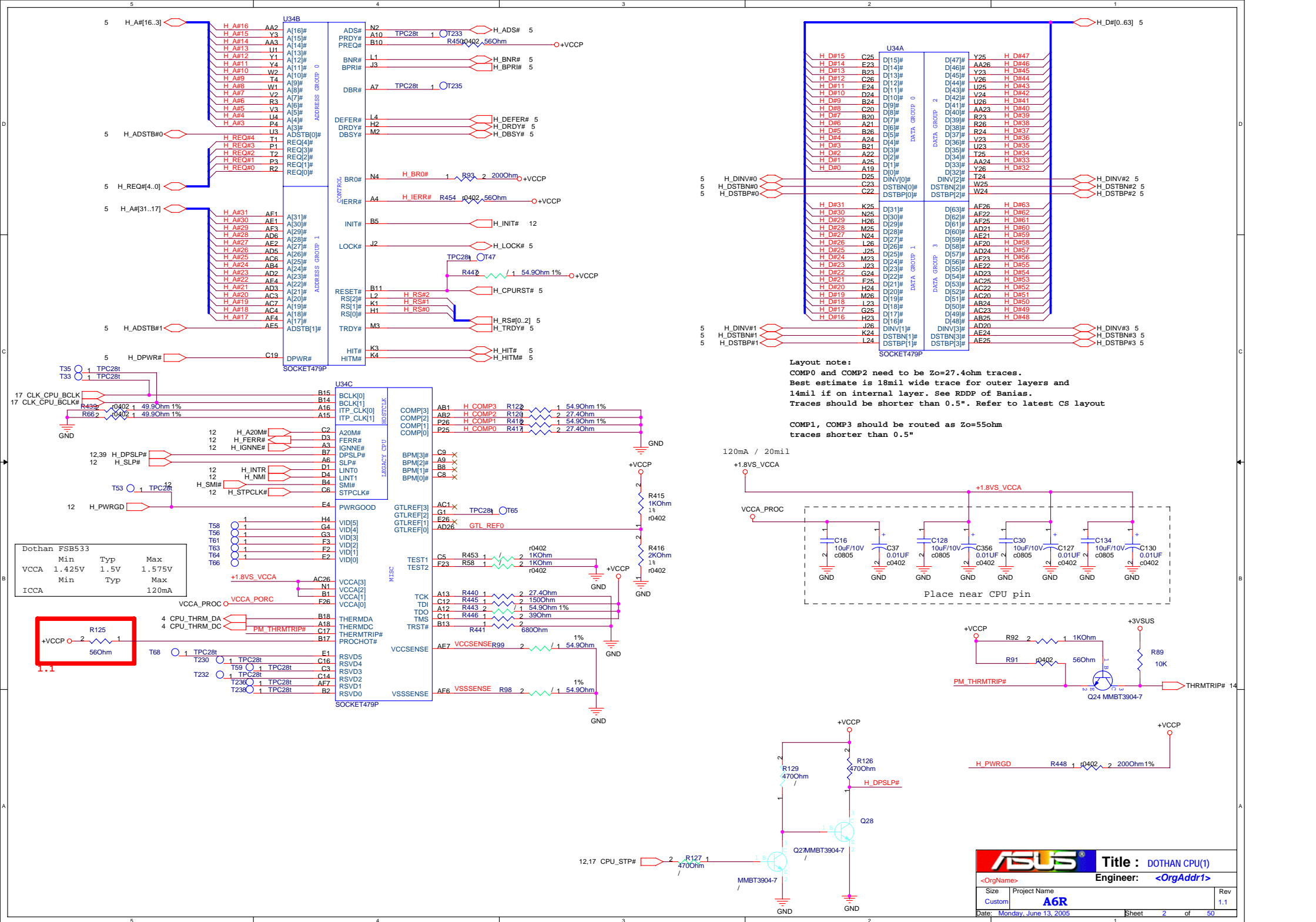
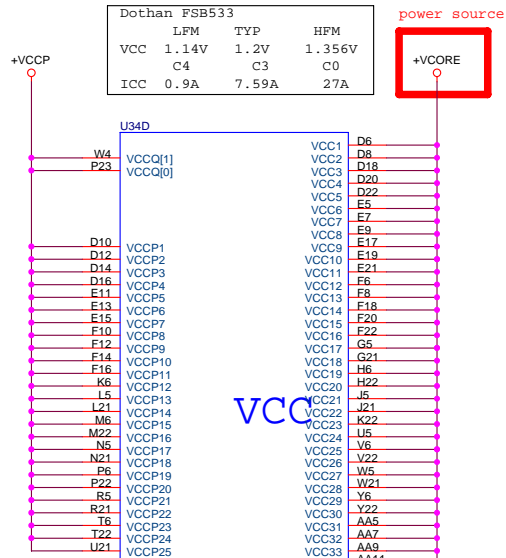


# CELERON/RC410MB/IXP400 BLOCK DIAGRAM







VCC

GND

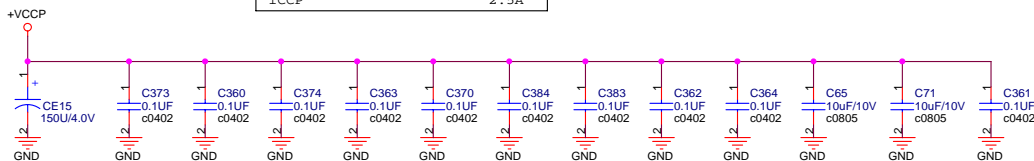
## MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

Dothan FSB533

	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
ICC			2.5A

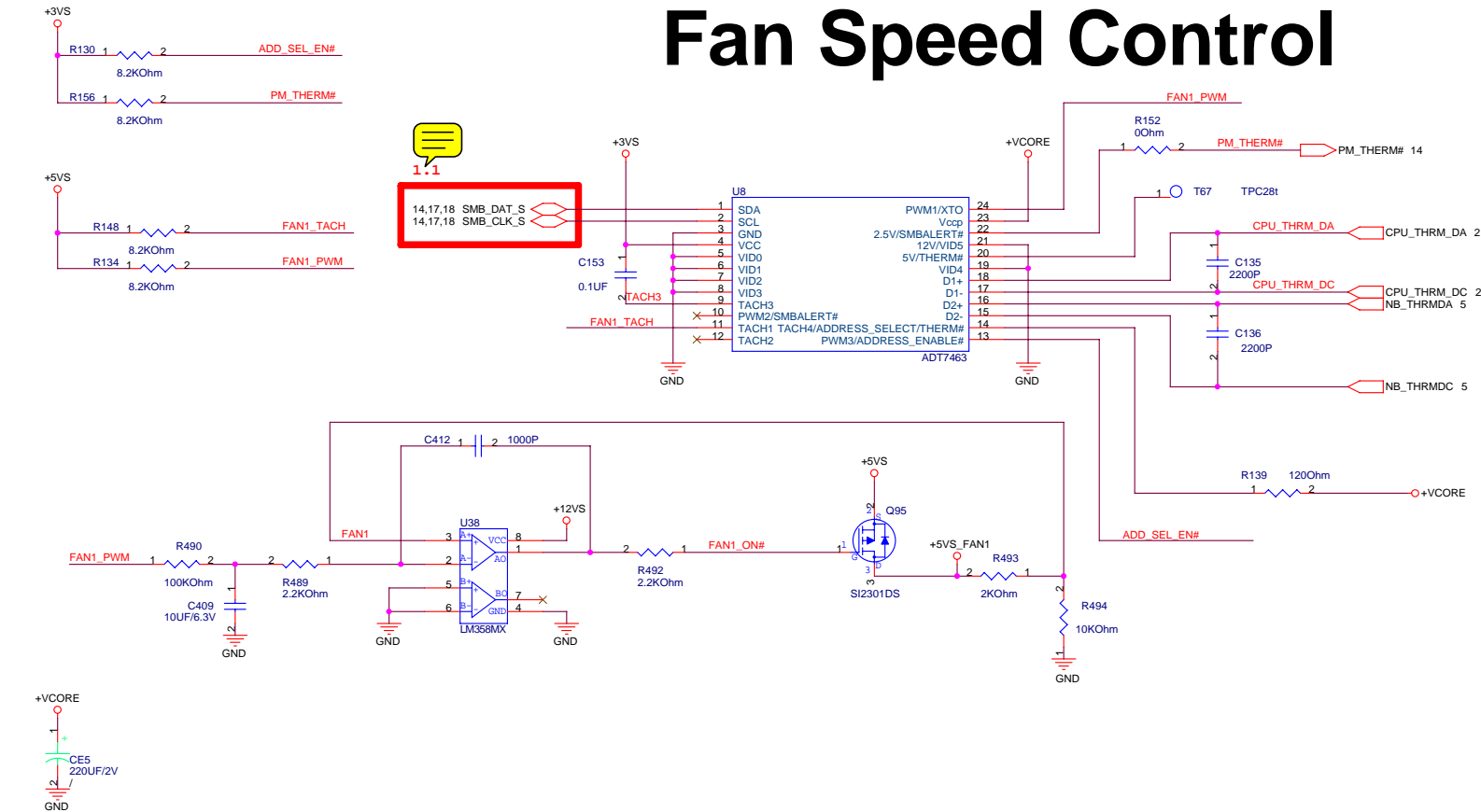
1.0V - 1.2V(+/- 5%)  
S0-S1M: 2.5  
A(CPU,MCH,ICH)



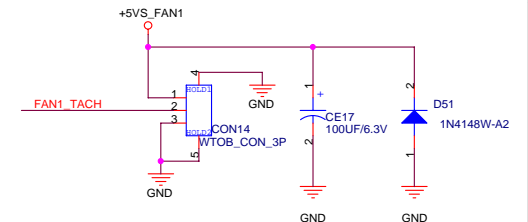
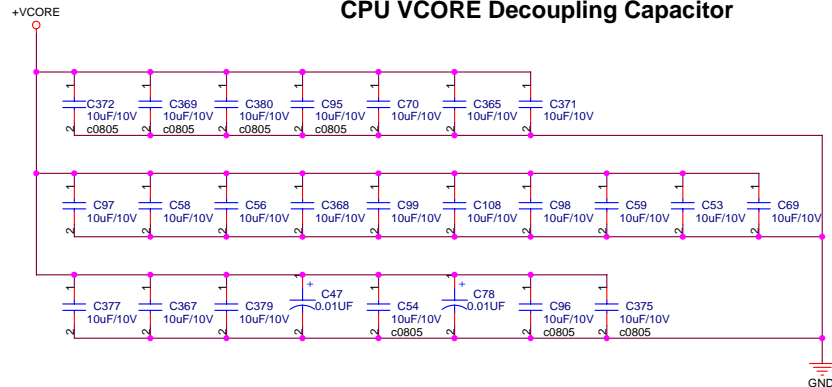
+VCCP (CPU) Decoupling Capacitor  
(Place near CPU)

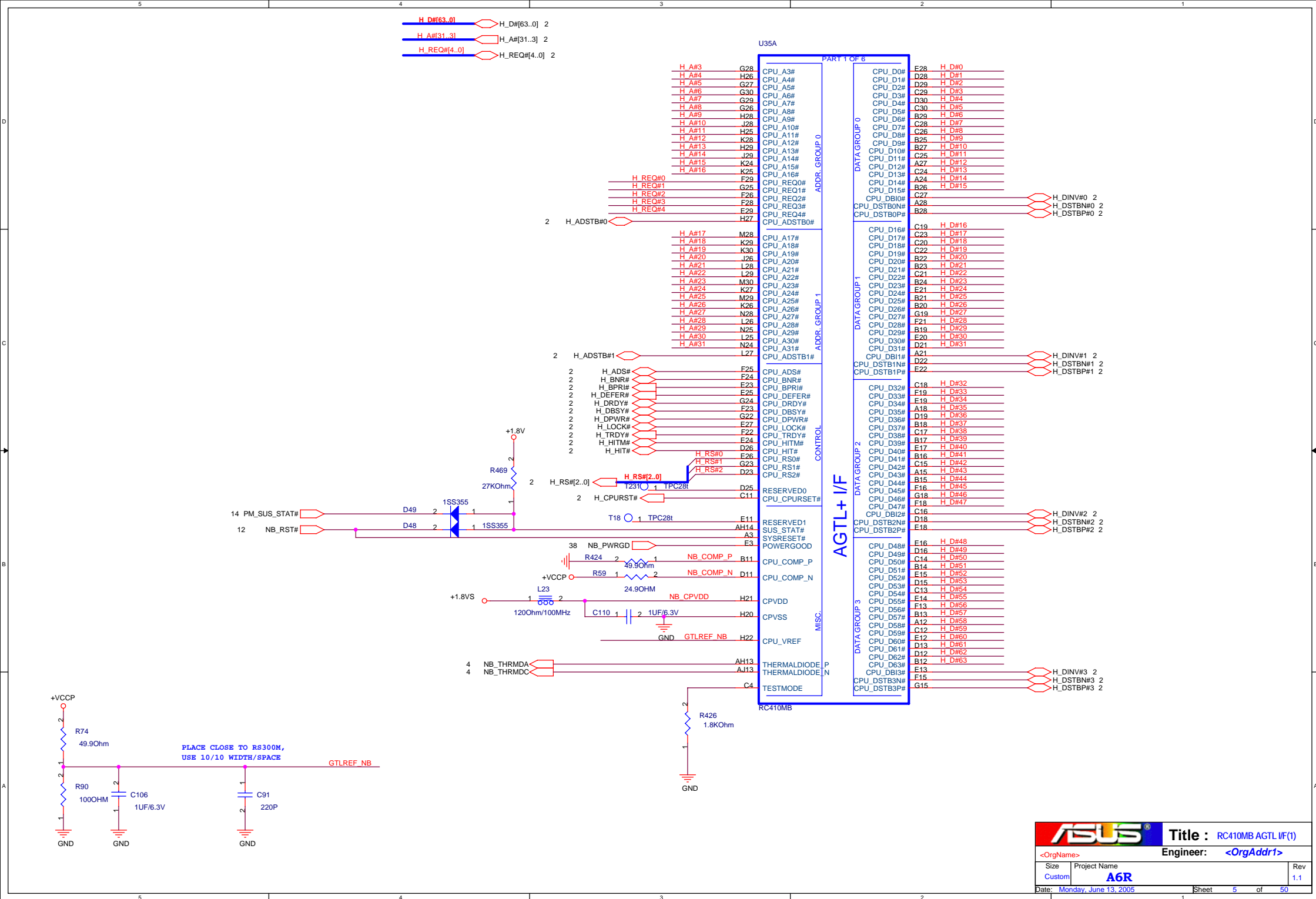
# Fan Speed Control

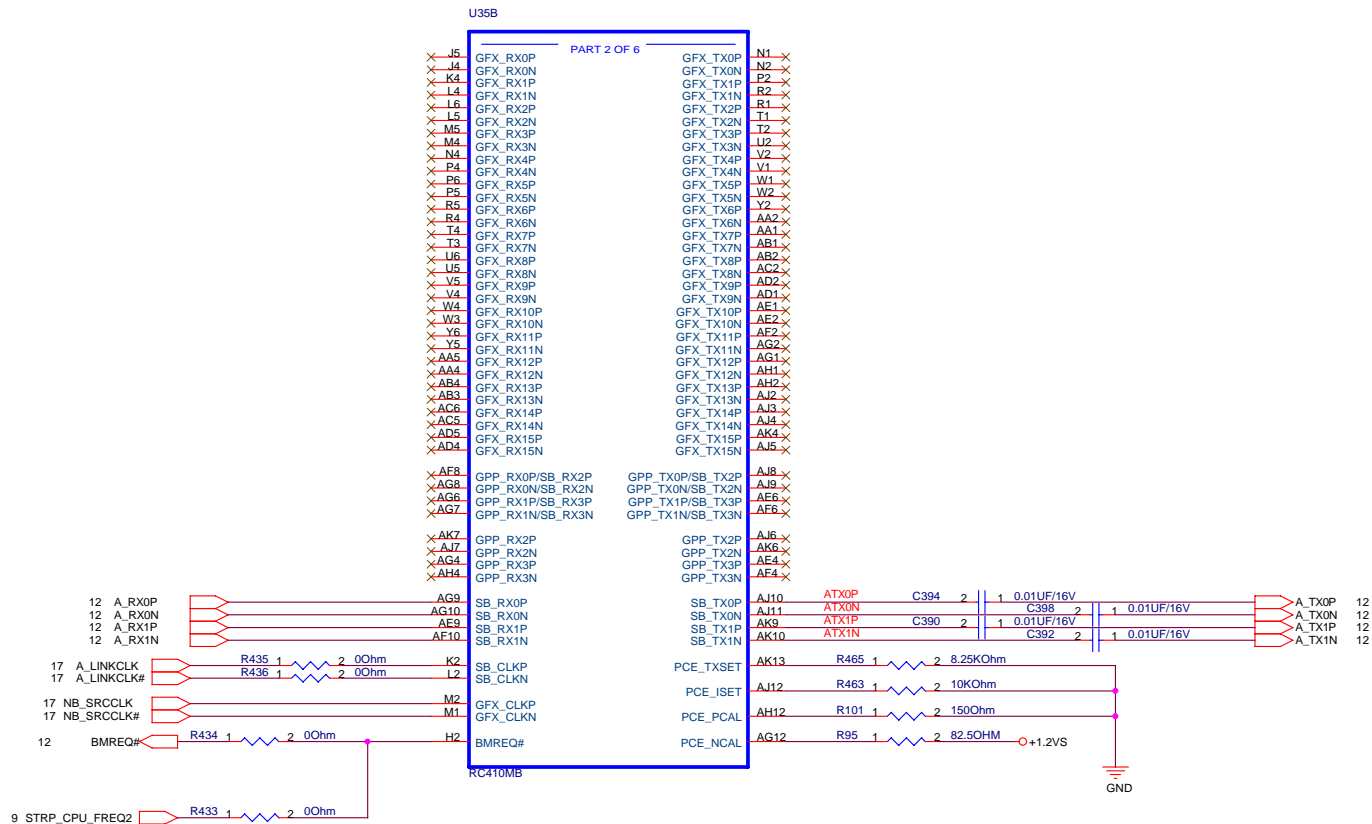
Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



## CPU VCORE Decoupling Capacitor



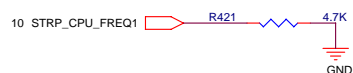
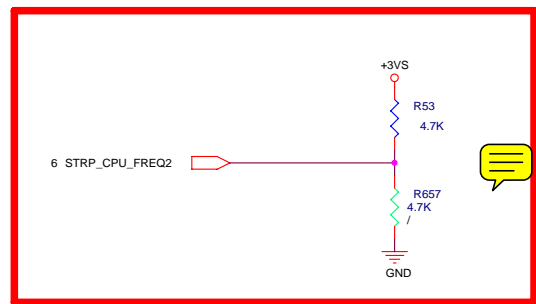










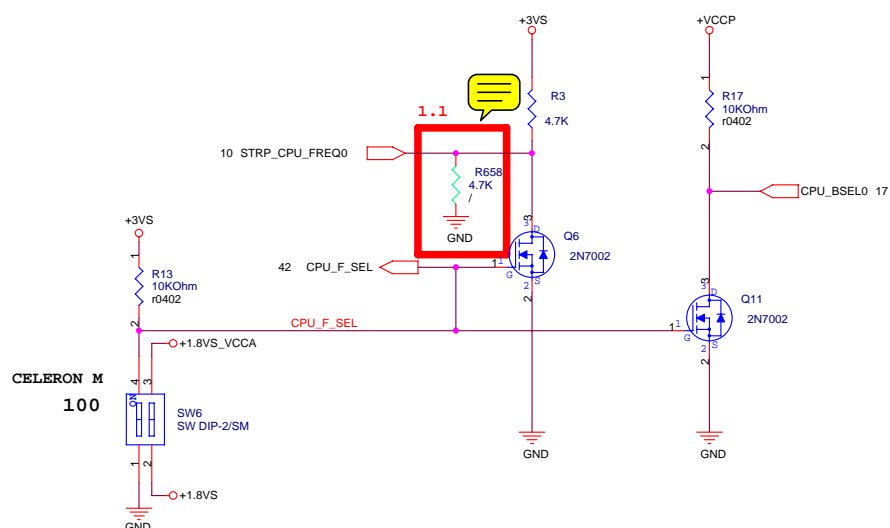
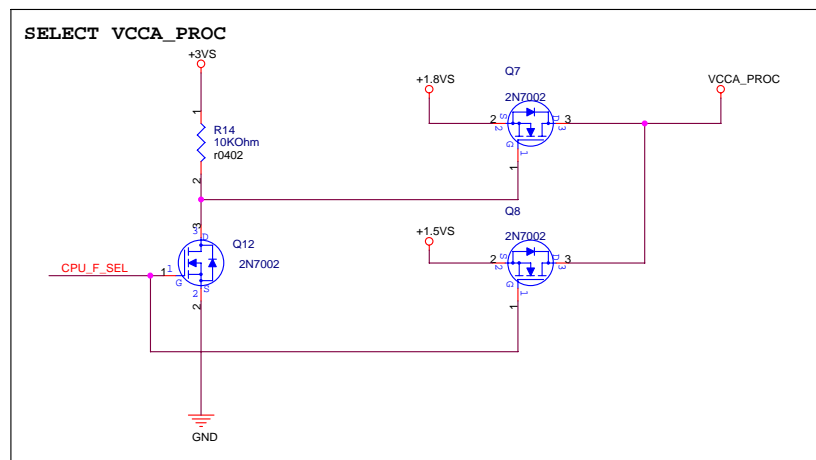


FSB	STRP_CPU_FREQ2	STRP_CPU_FREQ1	STRP_CPU_FREQ0
100MHZ	1	0	1
133MHZ	1	0	0
133MHZ	1	1	0
133MHZ	1	1	1
100MHZ	0	0	0
133MHZ	0	0	1
133MHZ	0	1	0
133MHZ	0	1	1

DEFAULT: 101

Note1: For A11, 100M and 133M need to strap at 101 or 001.

Note2: A12 changed 101 to be 100MHZ instead of 133MHZ in A11 ASIC.

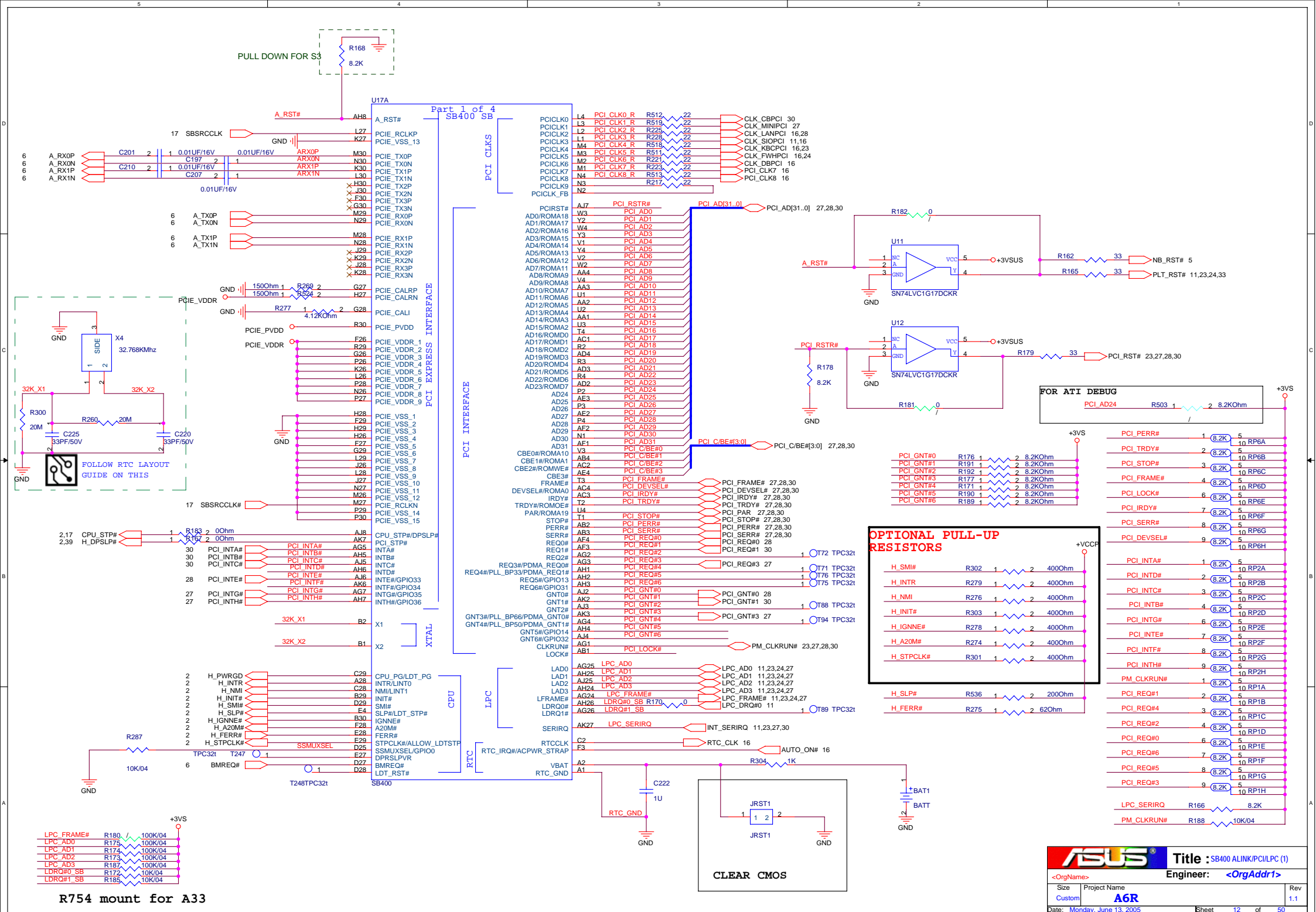


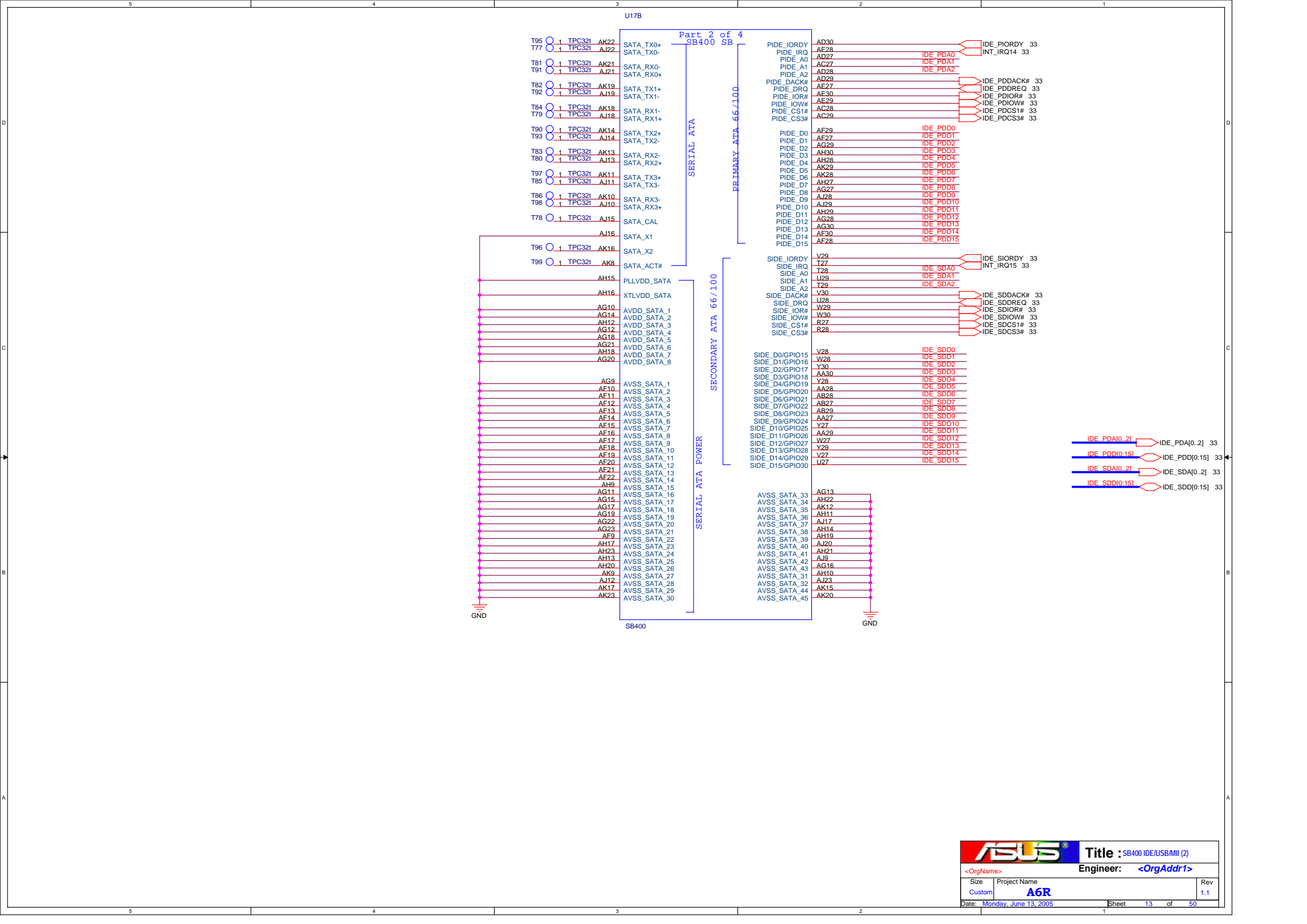
**SW8**  
**ON:** CPU\_F\_SEL=0 FSB100MHz VCCA\_PROC=1.8V  
**OFF:** CPU\_F\_SEL=1 FSB133MHz VCCA\_PROC=1.5V

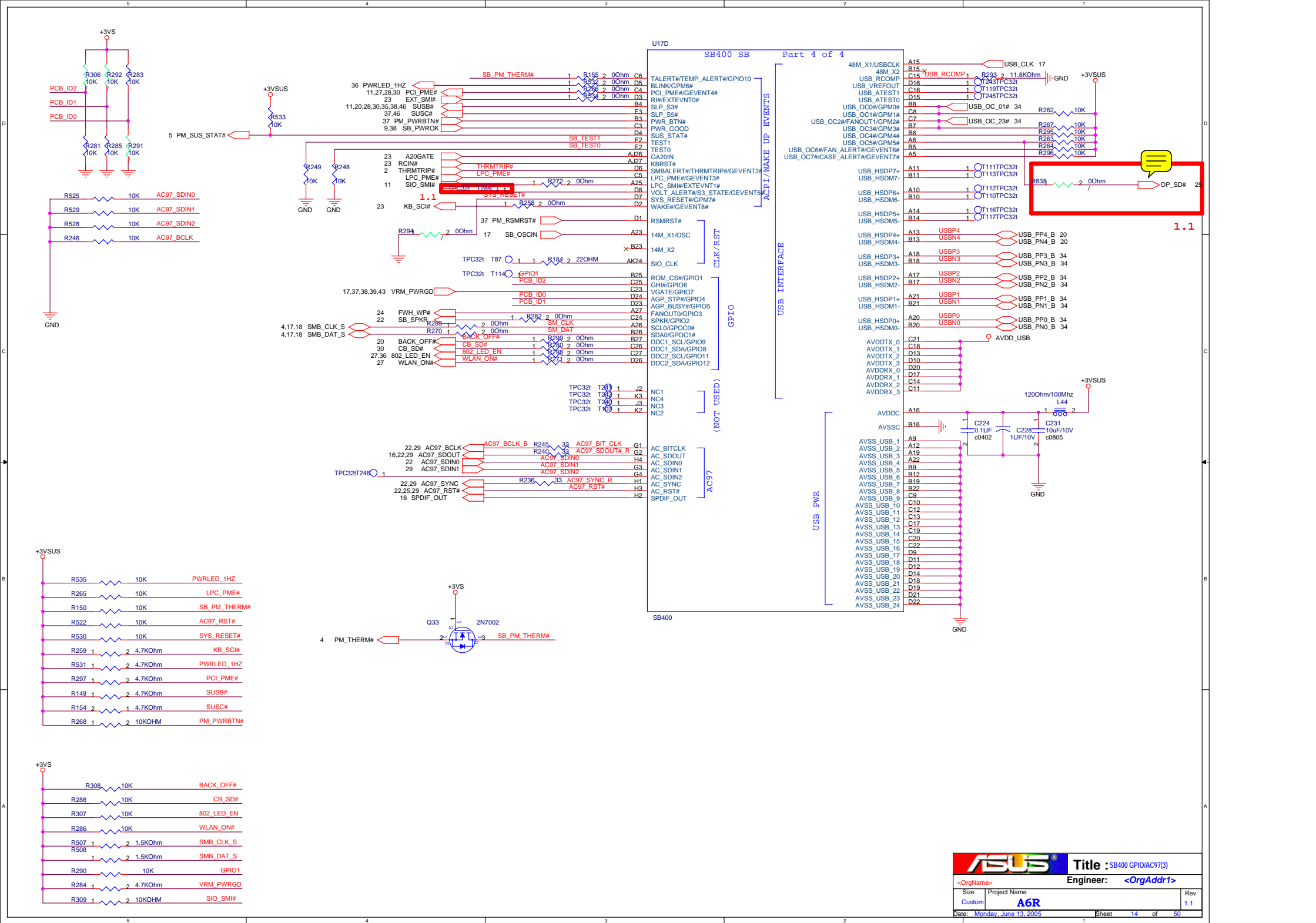
**STRP\_CPU\_VOLTAGE: CPU VCC**  
**0: MOBILE CPU**  
**1: DESKTOP CPU**  
**DEFAULT:0**





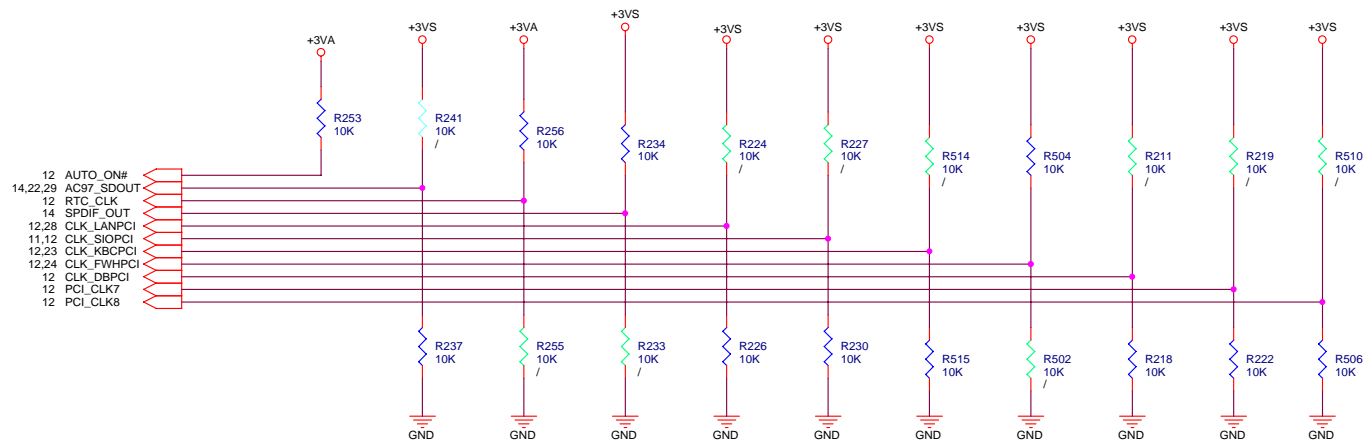








## REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7	PCI_CLK8
<b>PULL HIGH</b>	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz		USB PHY PWRDOWN DISABLE	USE USB PLL		CPU I/F = K8	ROM TYPE H,H = PCI ROM	
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712 )	SIO 48MHz	SEE NOTE1	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	SEE NOTE2	CPU I/F = P4	H,L = LPC ROM I <b>DEFAULT</b> LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM	

### NOTE

#### 1. USB CLK STRAPPING CHANGE

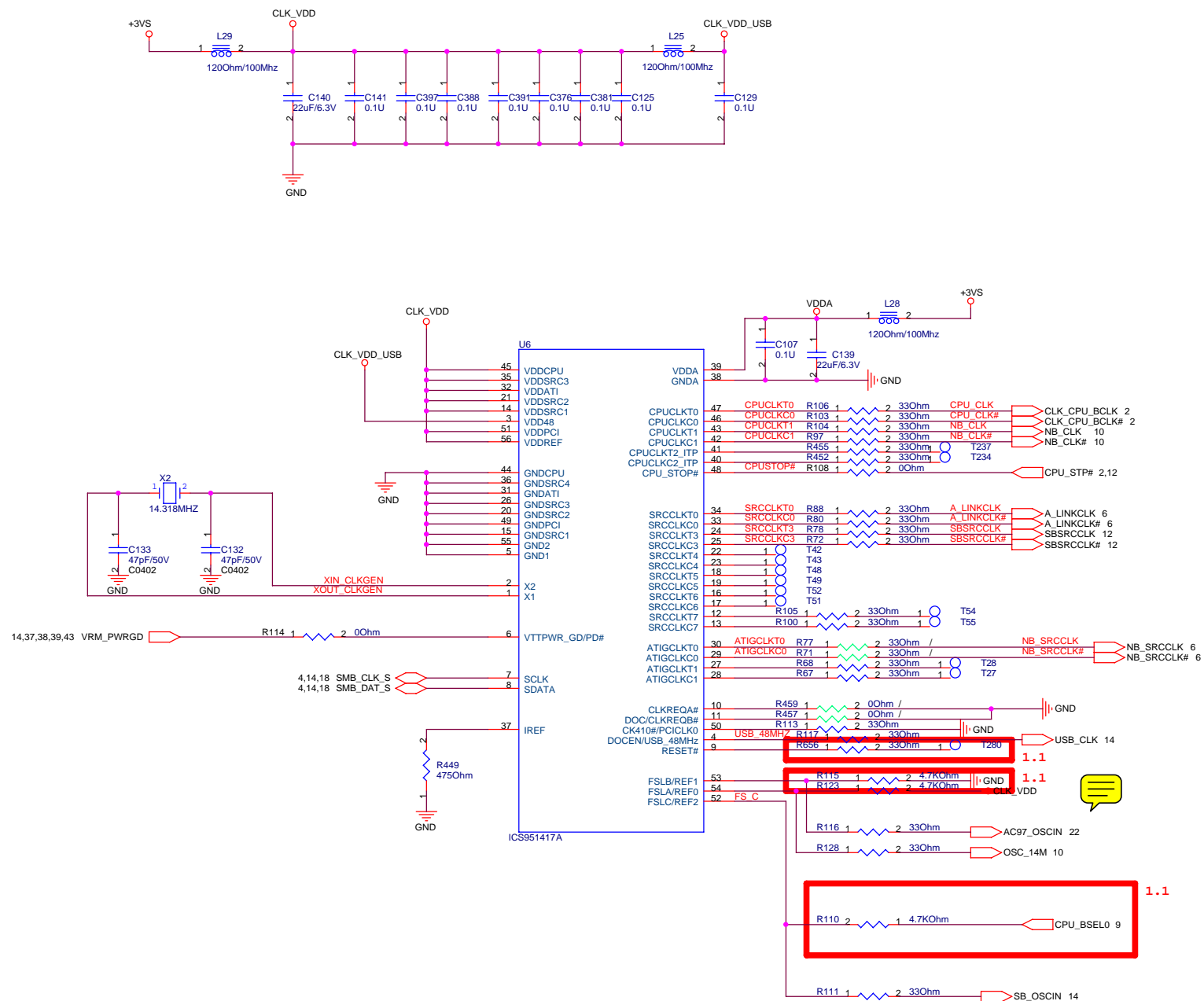
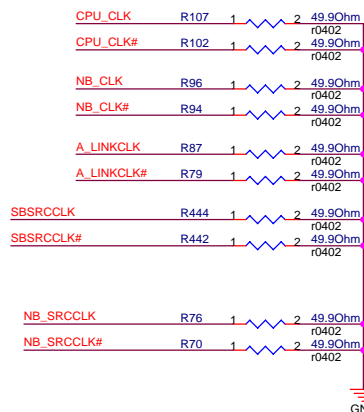
	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

#### 2. 14MHz CLOCK TYPE STRAPPING

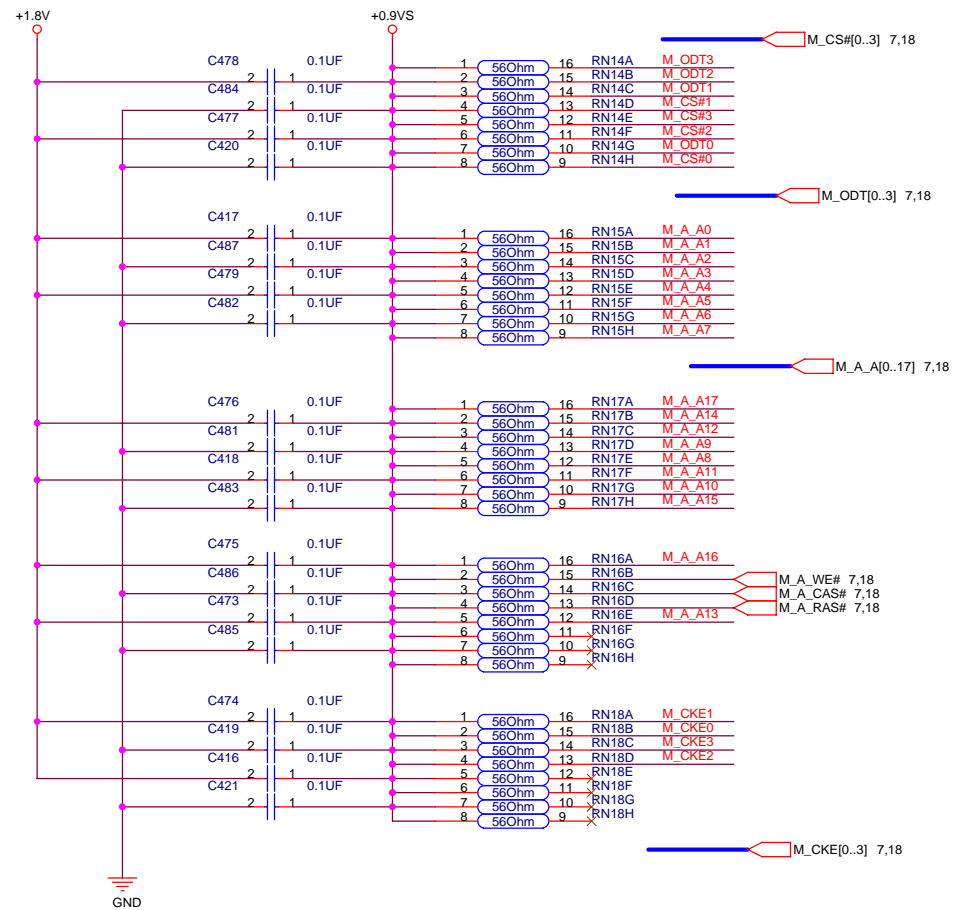
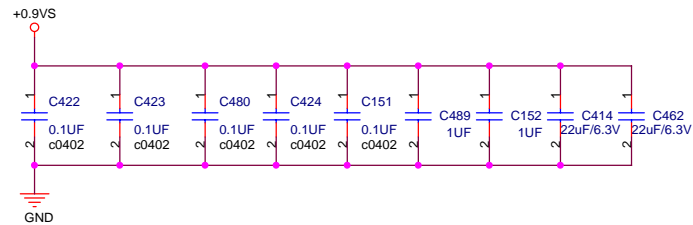
	A11-A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH



PLACE termination close to source IC

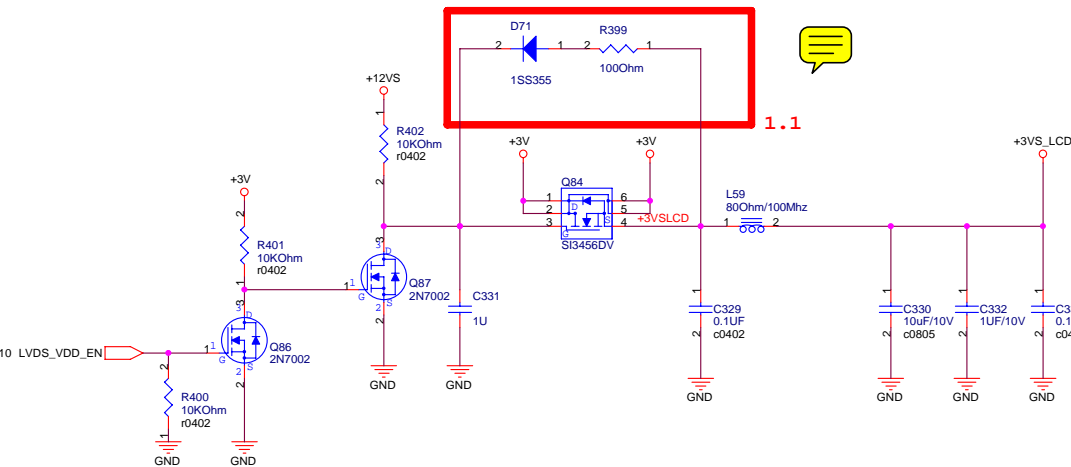




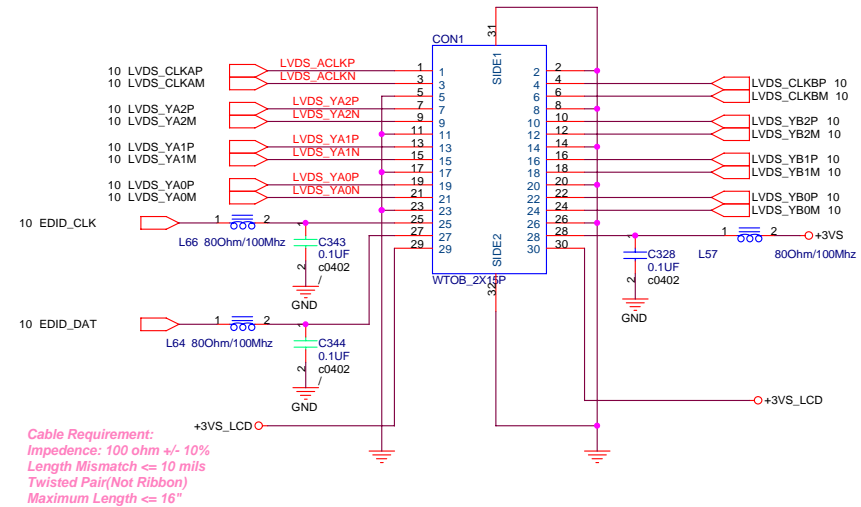


## LCD Power

3V-3.6V  
Full Active: 410 mA(Max. 500 mA)

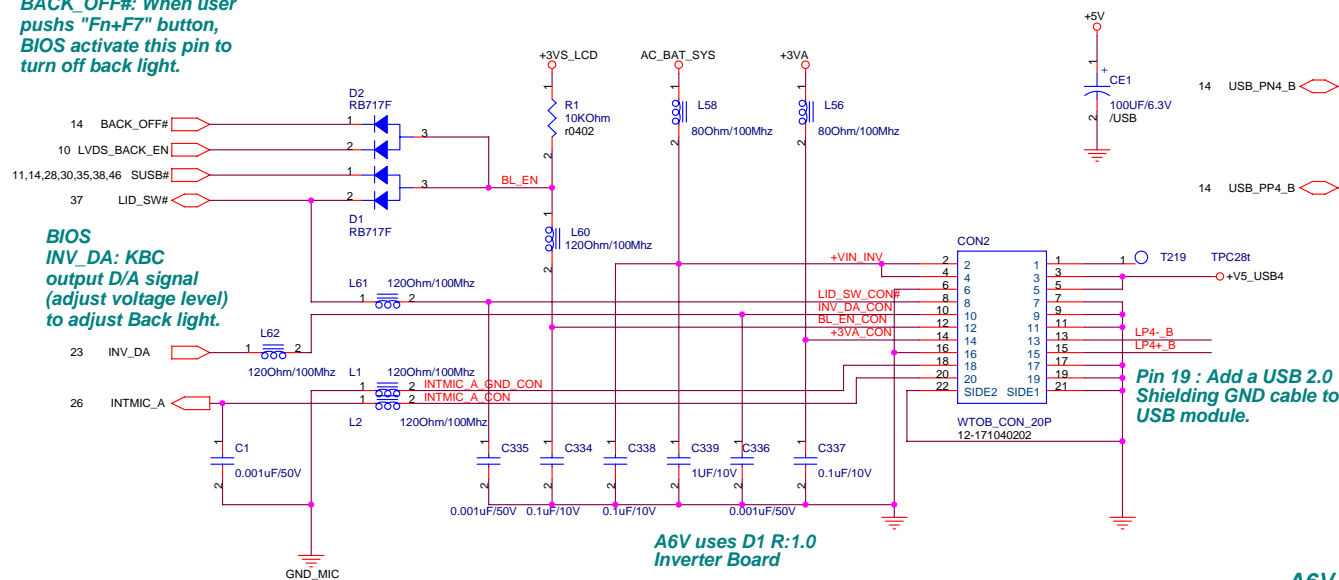


## LCD LVDS Interface



## INVERTER Interface

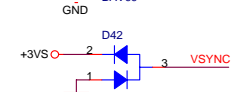
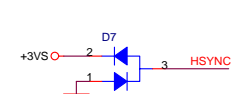
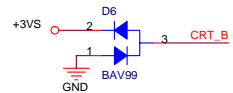
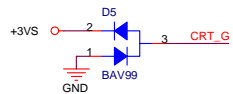
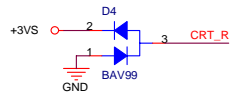
**BIOS BACK\_OFF#:** When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.



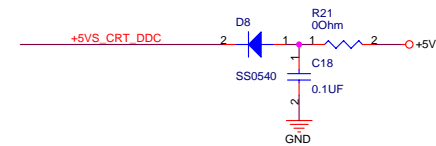
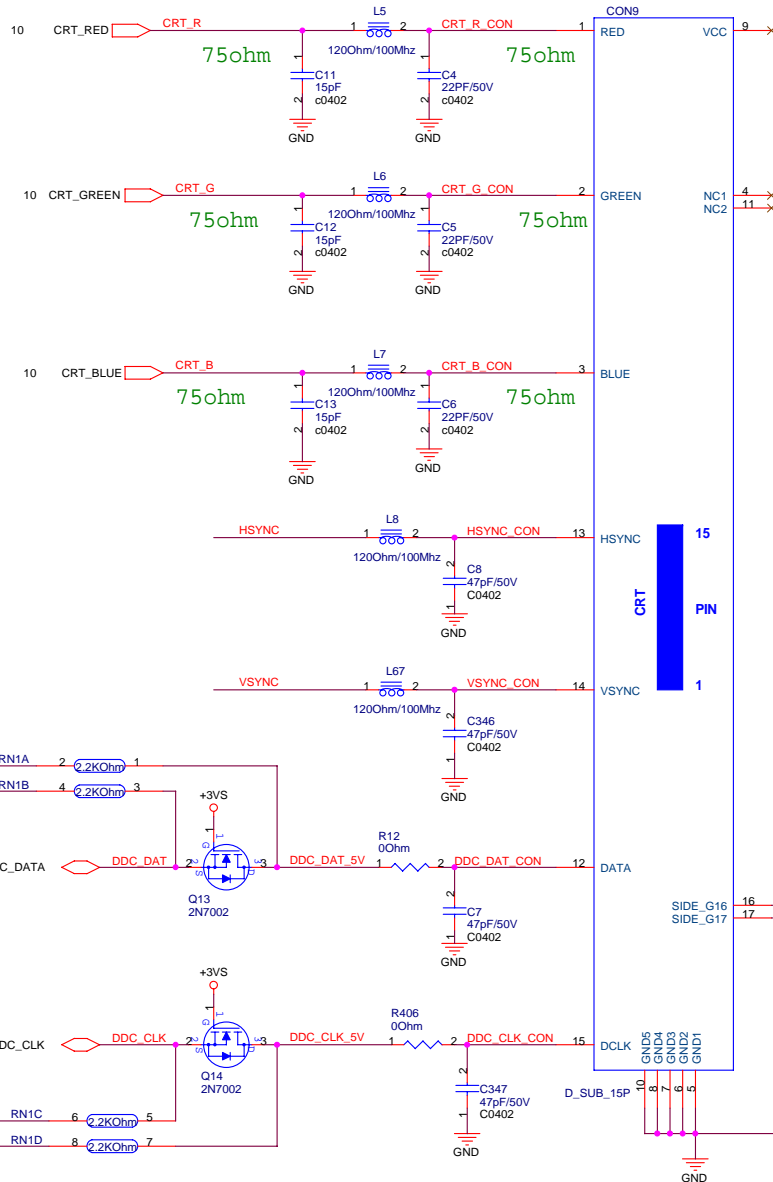
## USB PORT 4 for USB CAMERA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

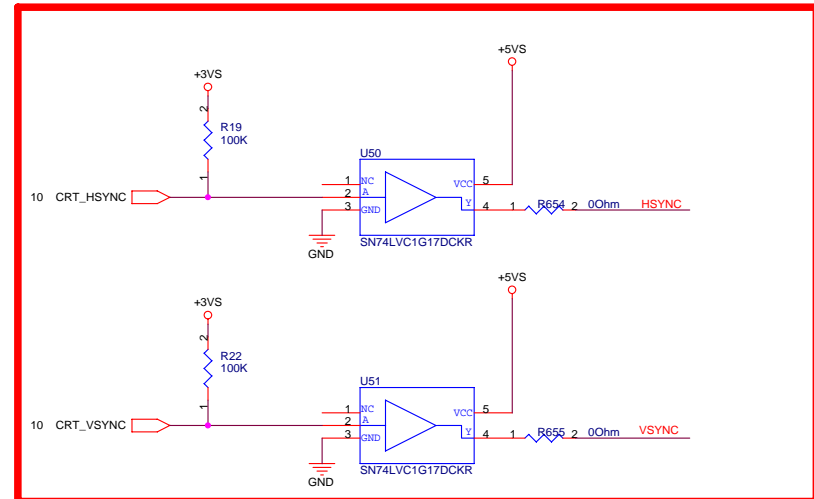
A6V doesn't support USB WLAN function!

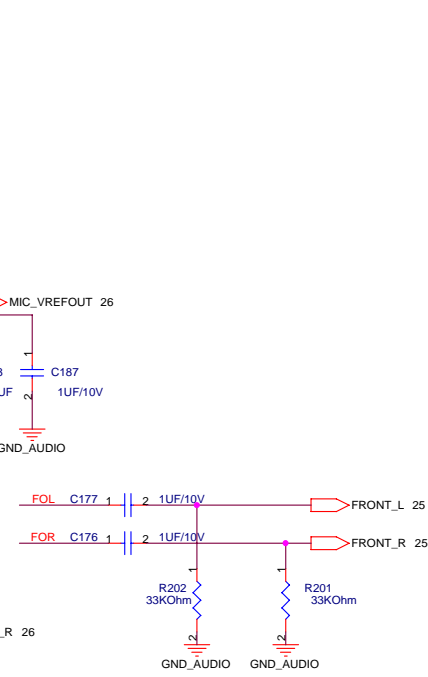
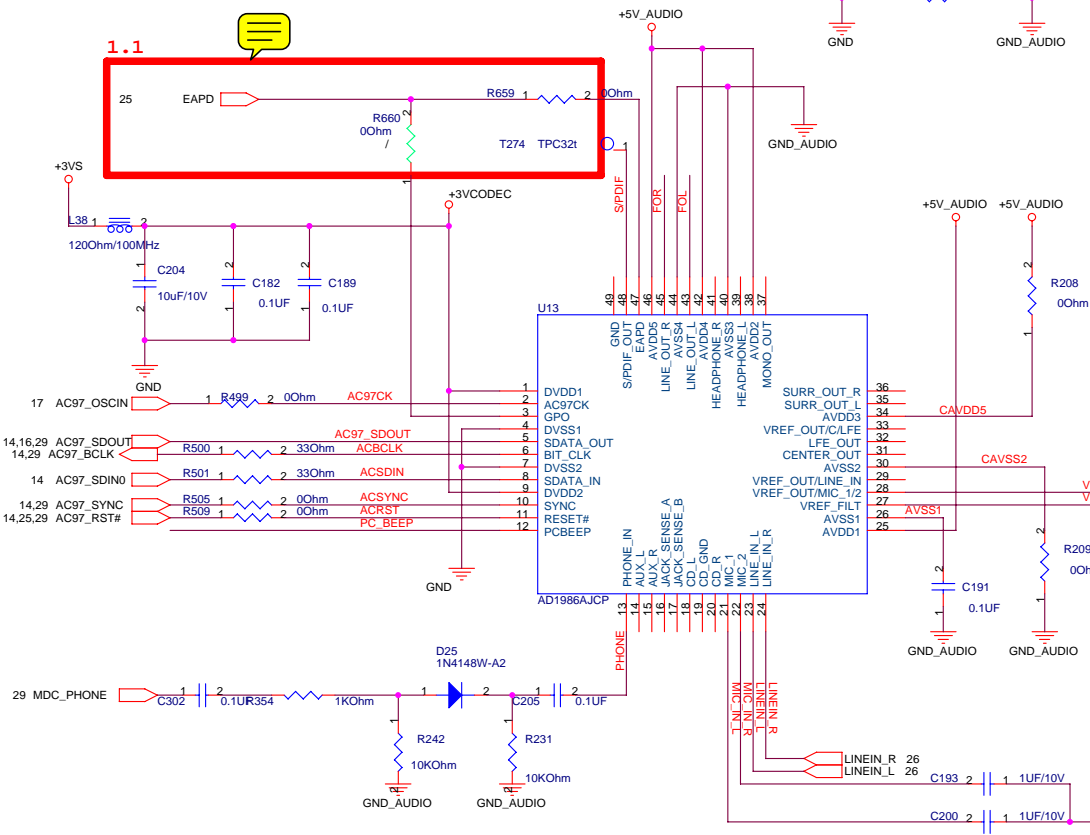
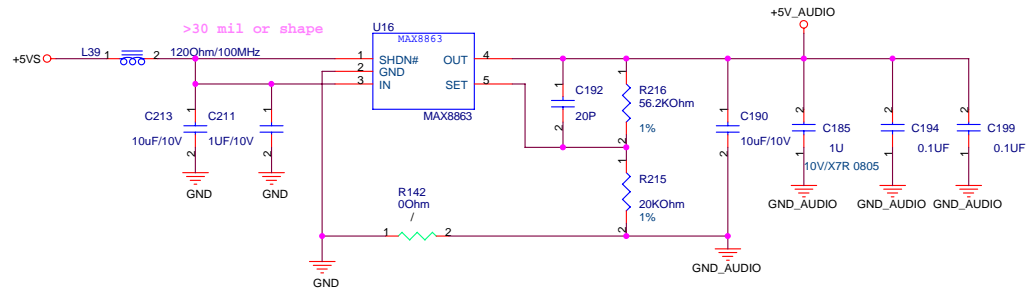
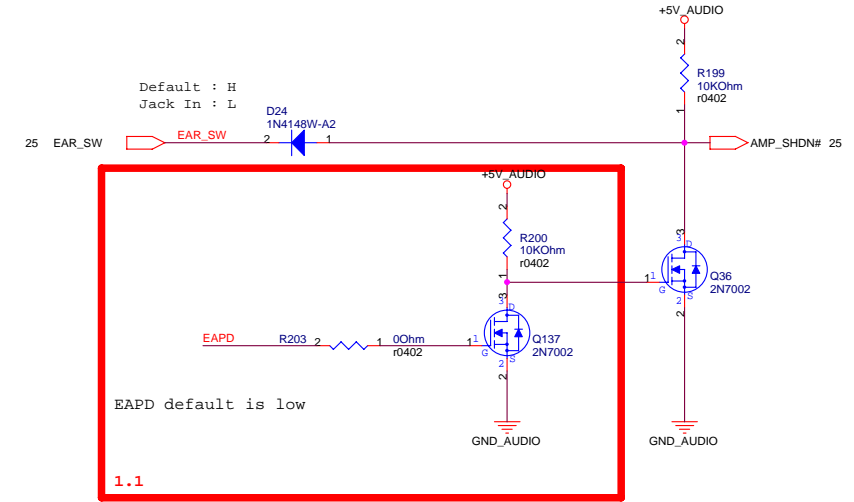
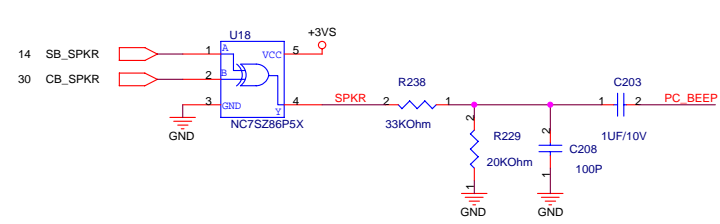


PLACE ESD  
Diodes near  
VGA port



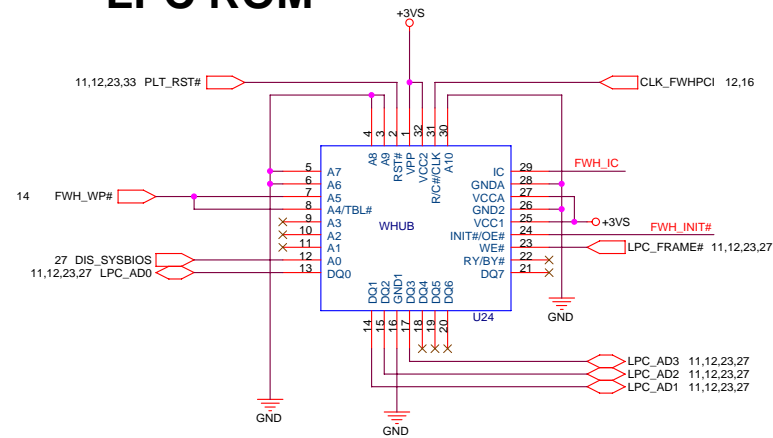
1.1



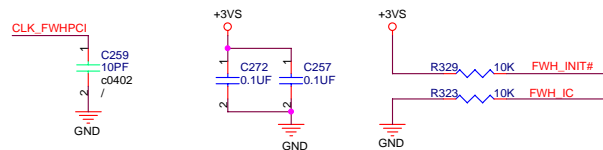




# LPC ROM

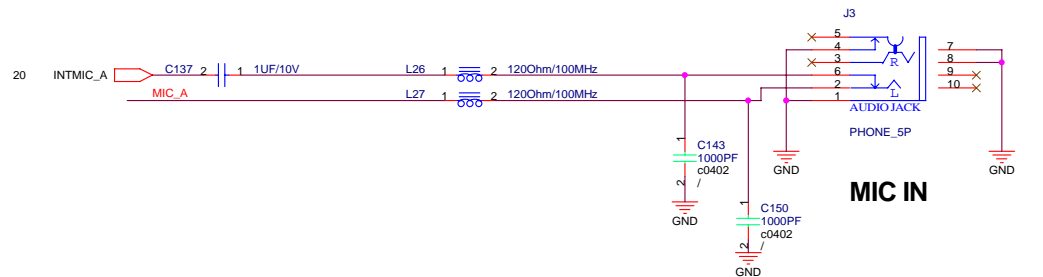


PLCC32 Socket Part Number :  
12-043000321  
SST FWH/LPC Part Number :  
05-001017122(曉)

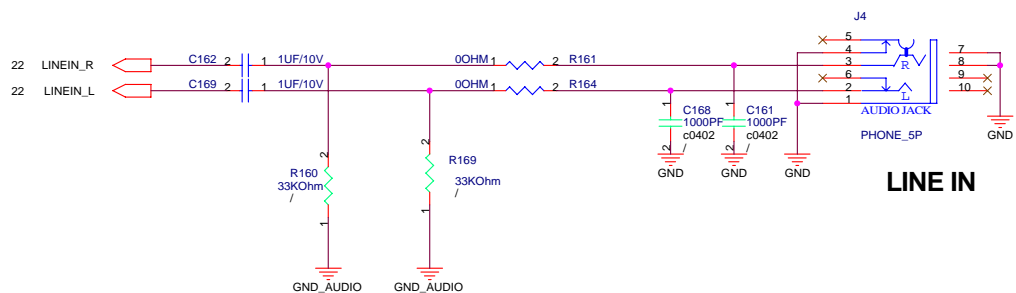
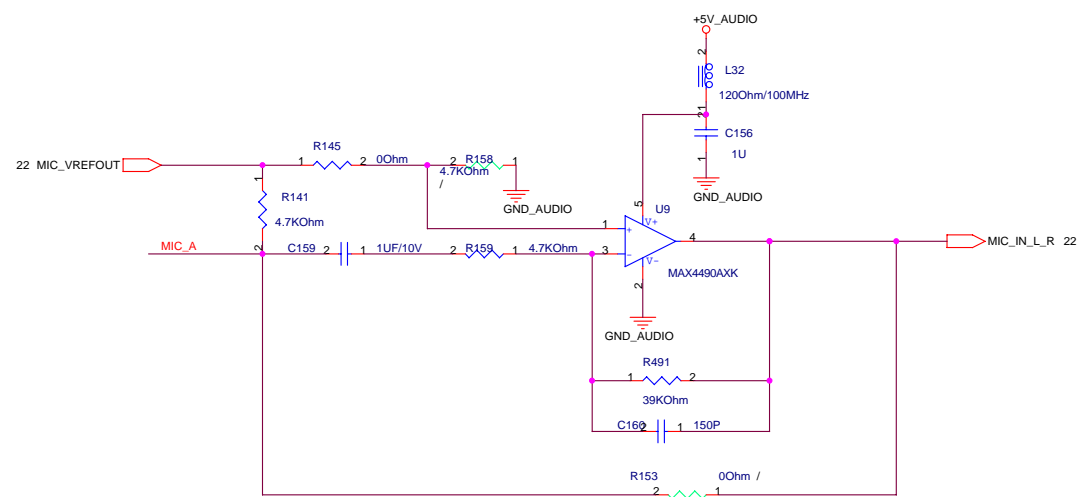
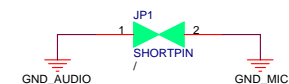


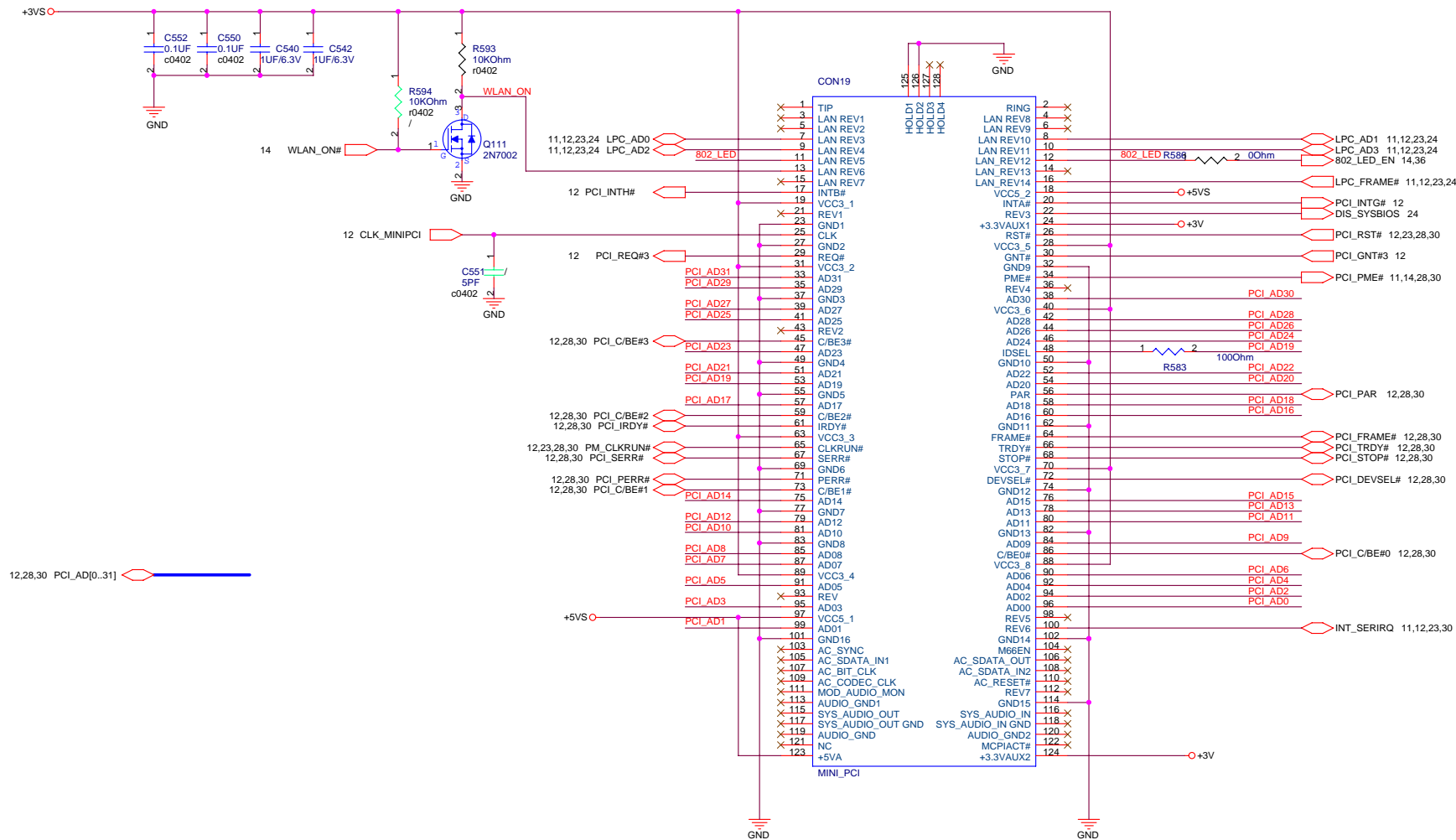




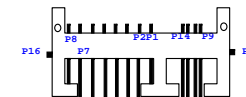
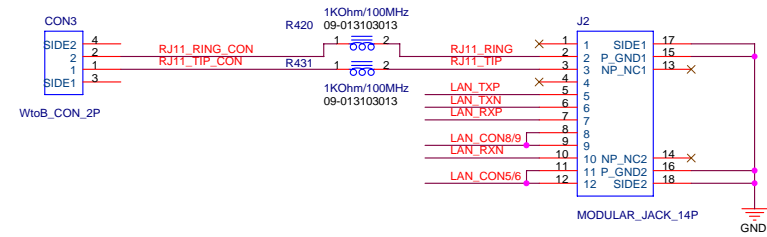
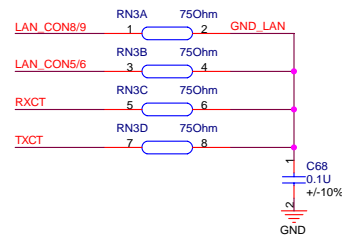
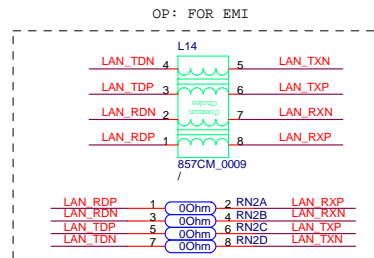
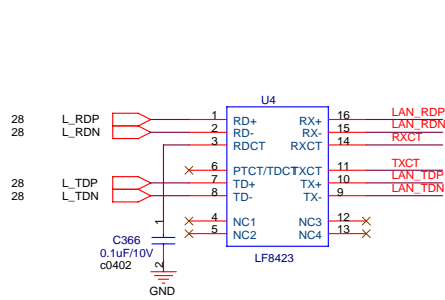


INTMIC\_A:GND\_AUDIO  
: W/P/X = 12/5/15mils





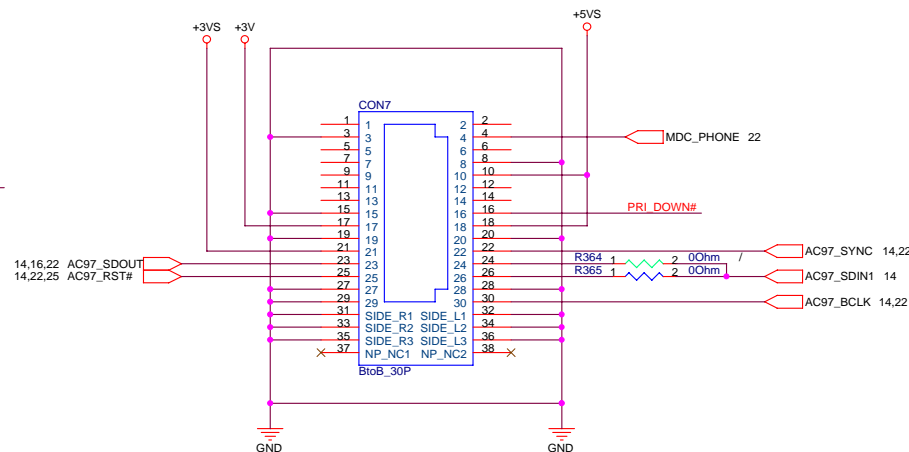
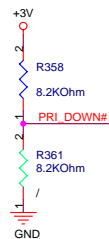
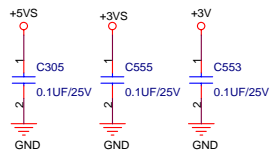


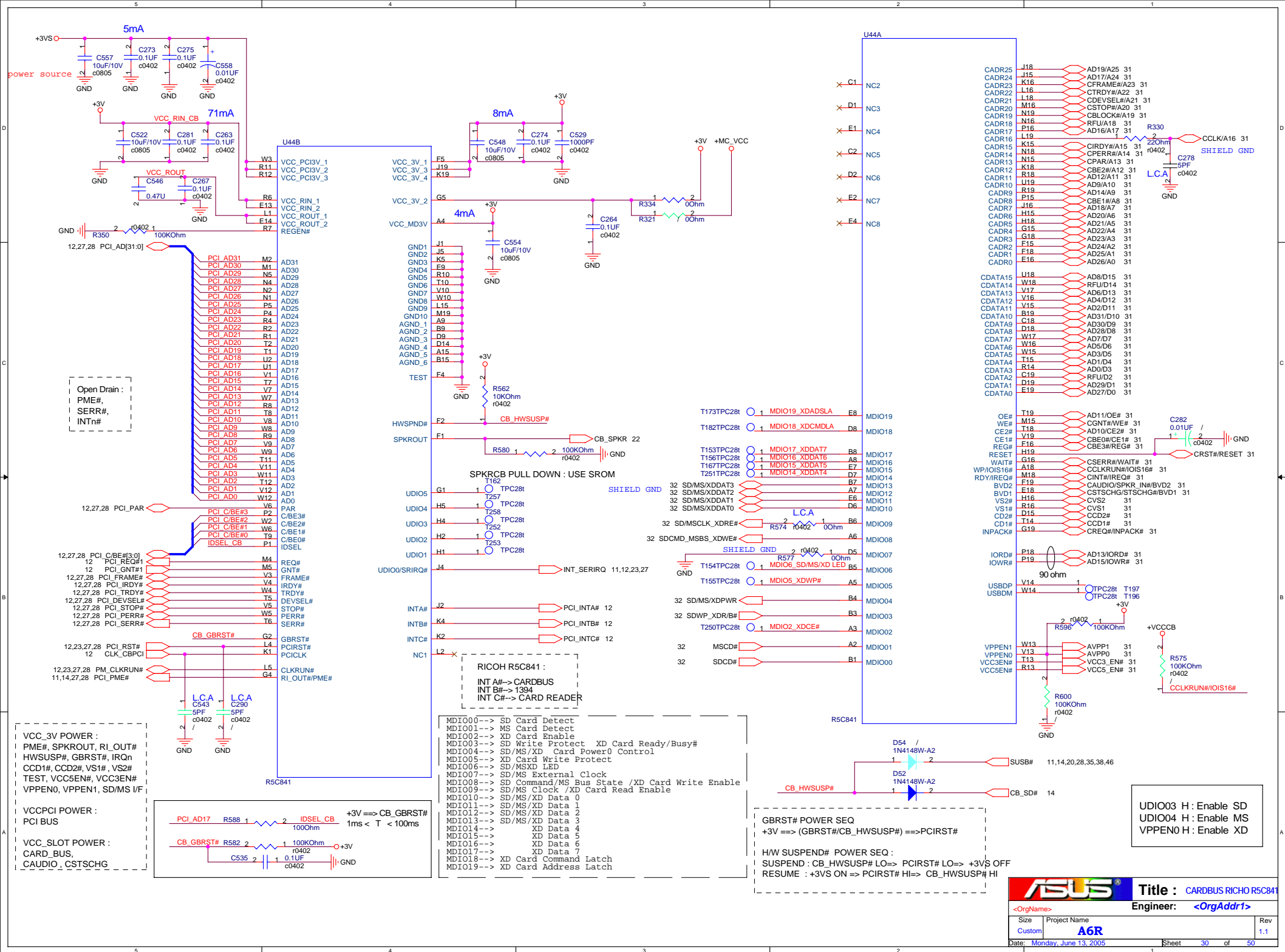


RJ 45 & RJ 11  
BOTTOM VIEW

## LAN PORT

## MDC



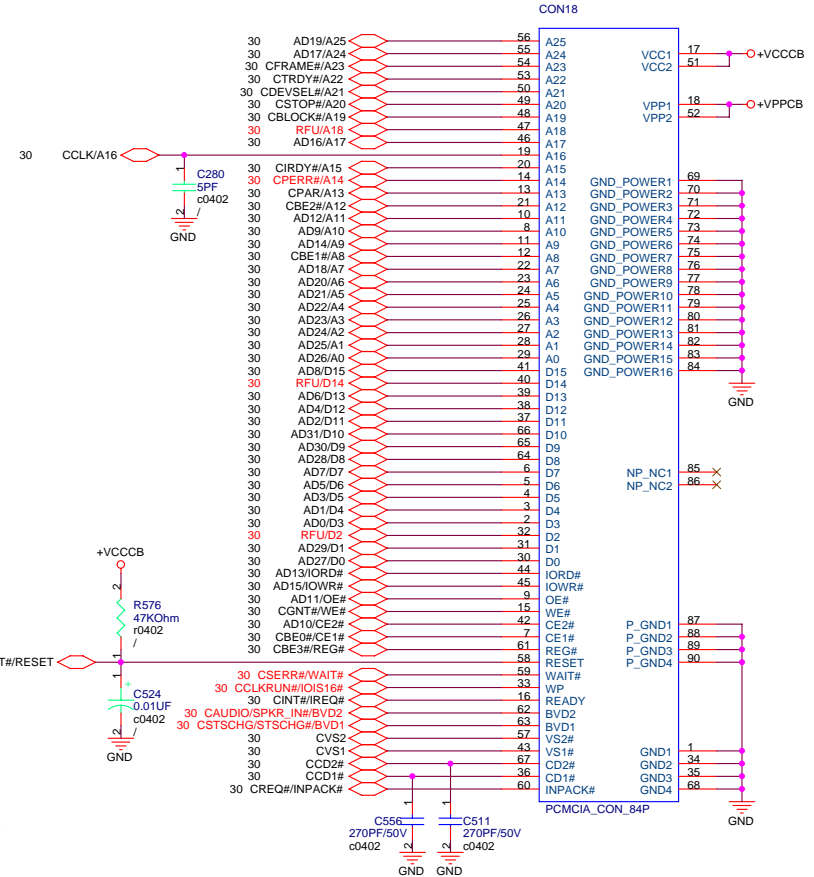
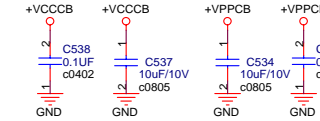
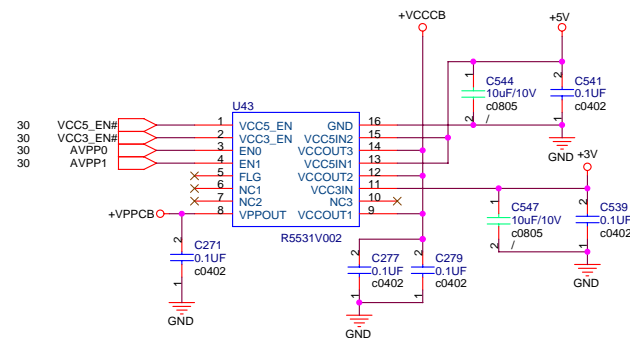
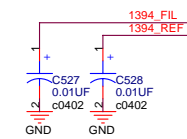
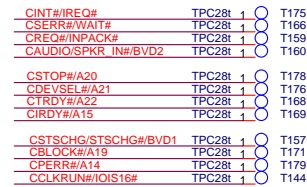
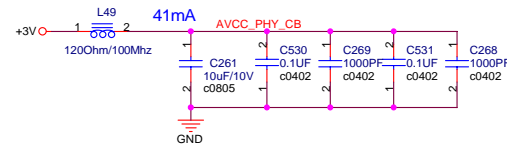
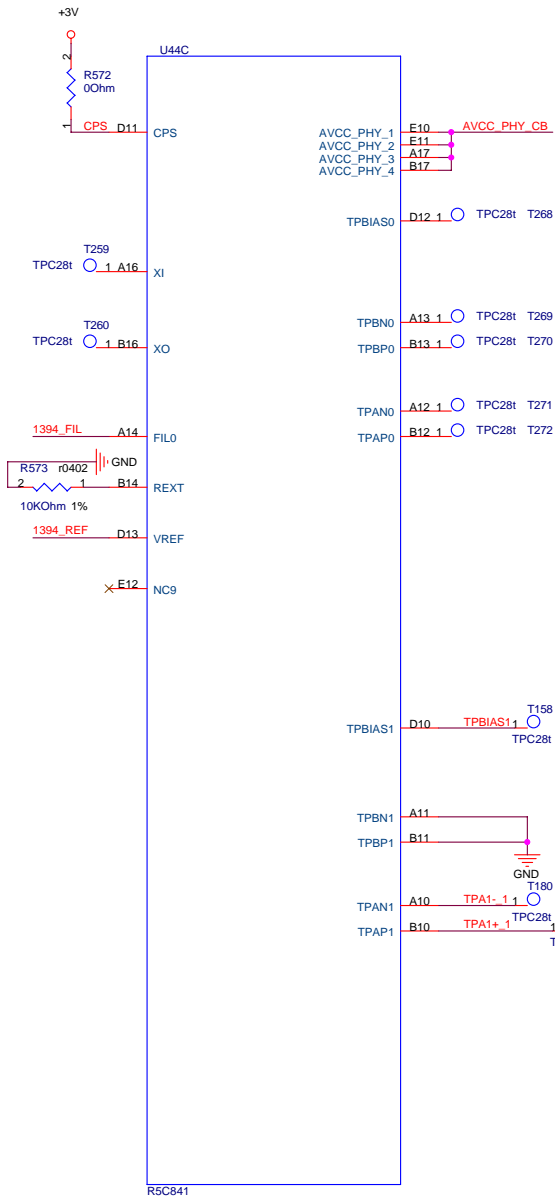


1.1

1394 crystal

Delete

X6 , C525 , C526



PCMCIA



Title : PCMCIA SOCKET

&lt;OrgName&gt; Engineer: &lt;OrgAddr1&gt;

Size Project Name

Custom A6R

Date: Monday, June 13, 2005 Sheet 31 of 50

Rev 1.1

## 1394 CON

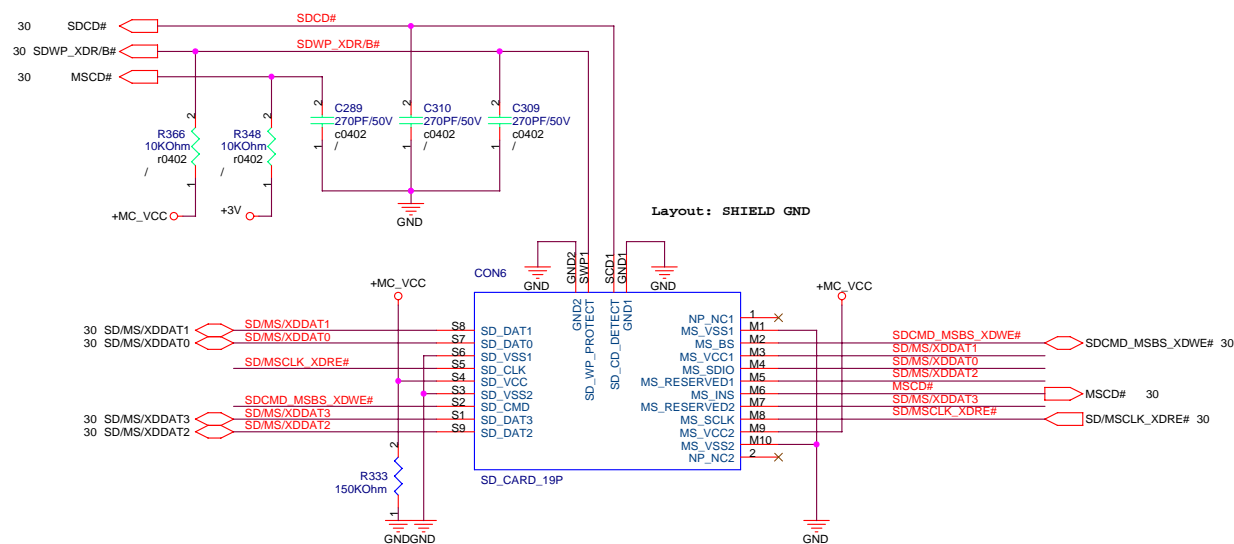
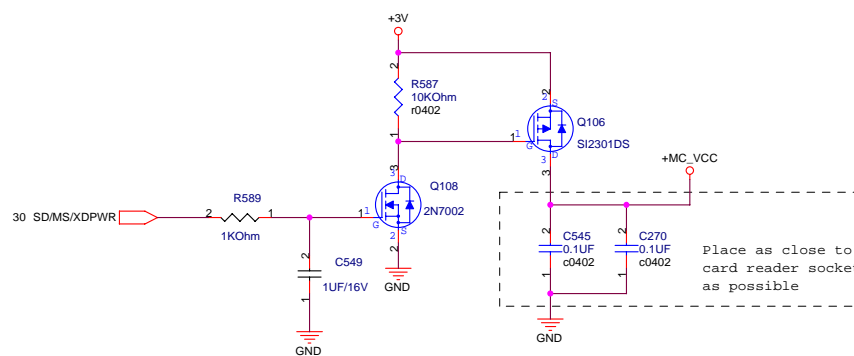
Delete

CON17 , L40 , R568 , R569

**R570 , R571 , R566 , C518**

C520 , C52

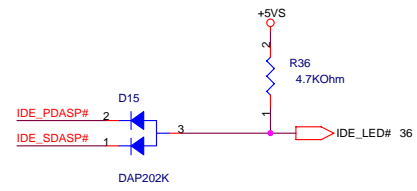
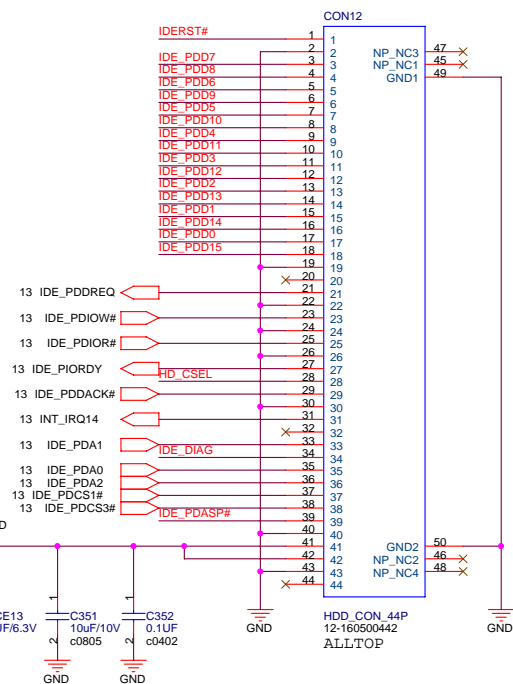
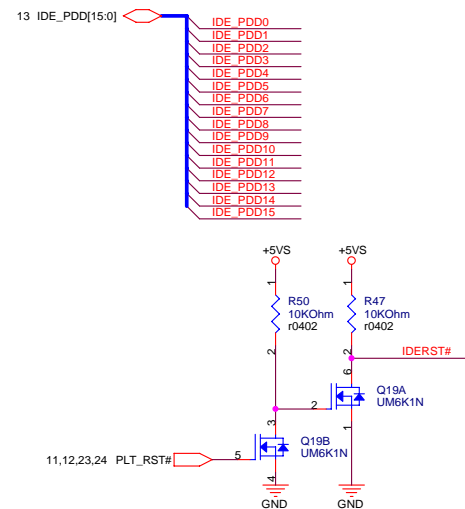
U42 , C532 , R579 , R584



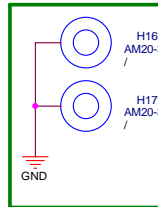
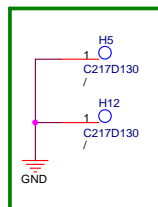
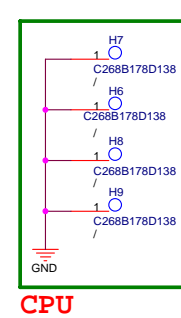
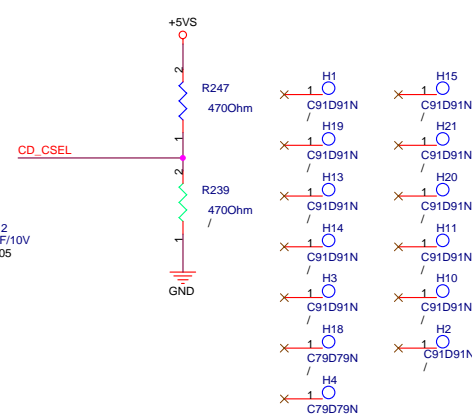
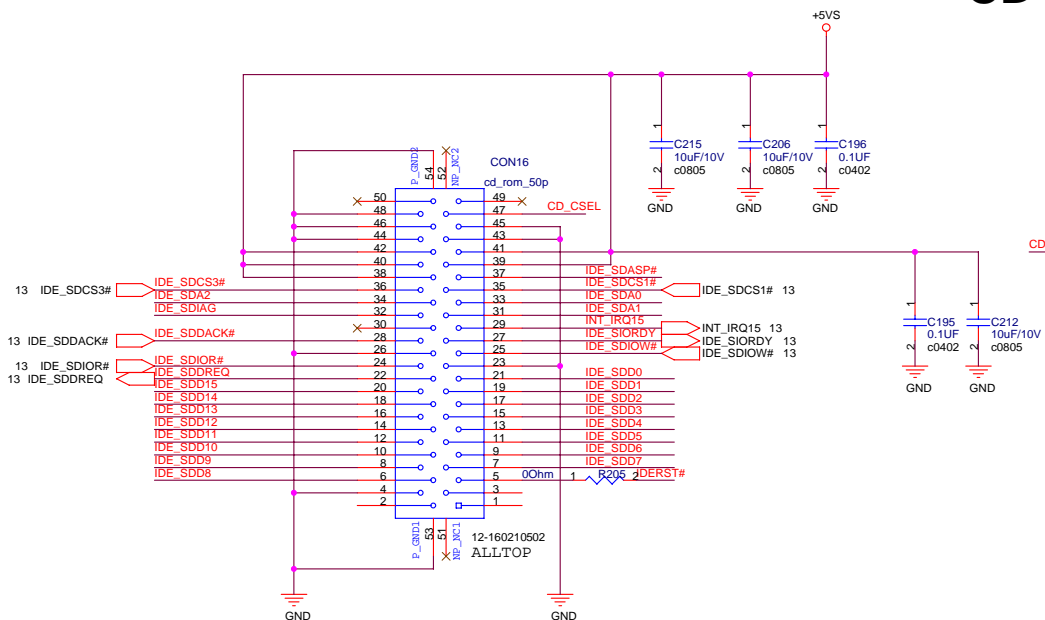


The diagram shows the electrical connections for the IDE pins on the Raspberry Pi 4. Three red lines represent the IDE\_SDIAG, IDE\_DIAI, and HD\_CSEL pins. Each line has a resistor connected to a +5V source and another resistor connected to ground. The ground is labeled GND.

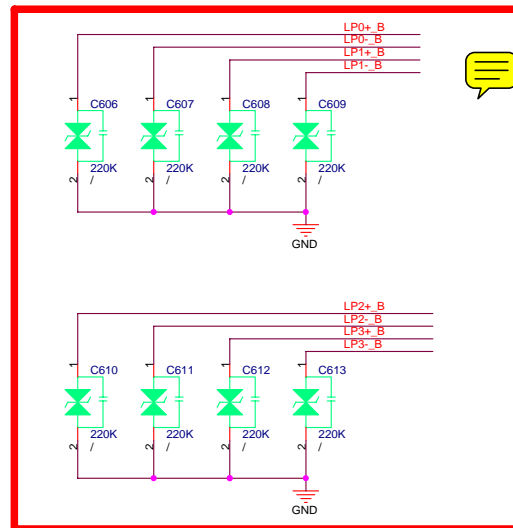
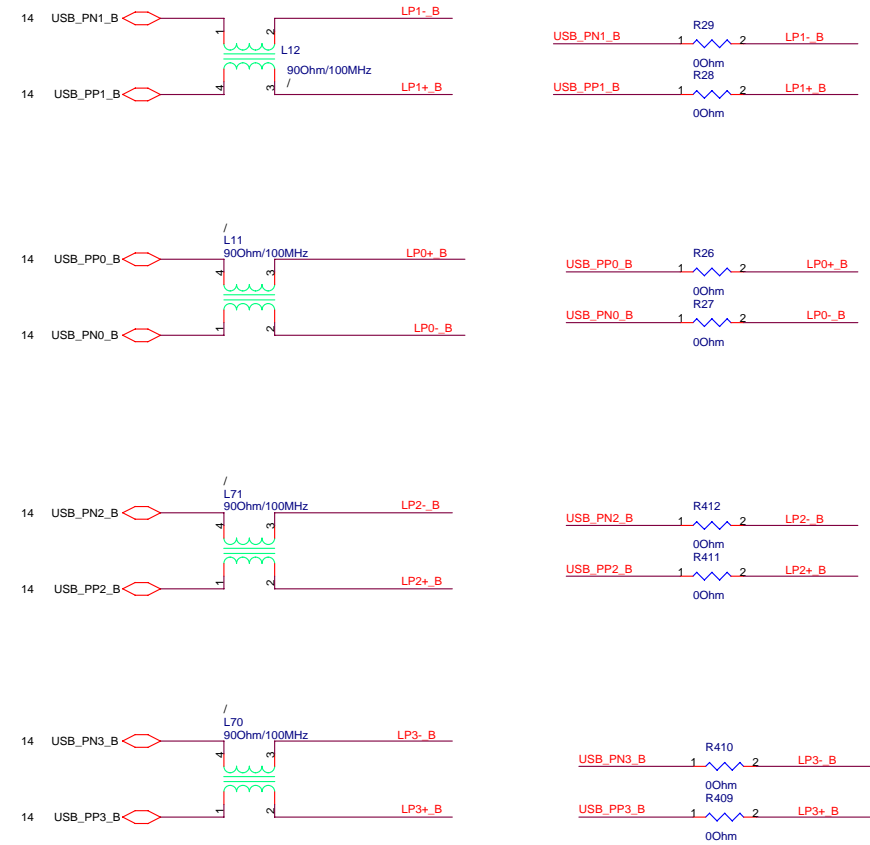
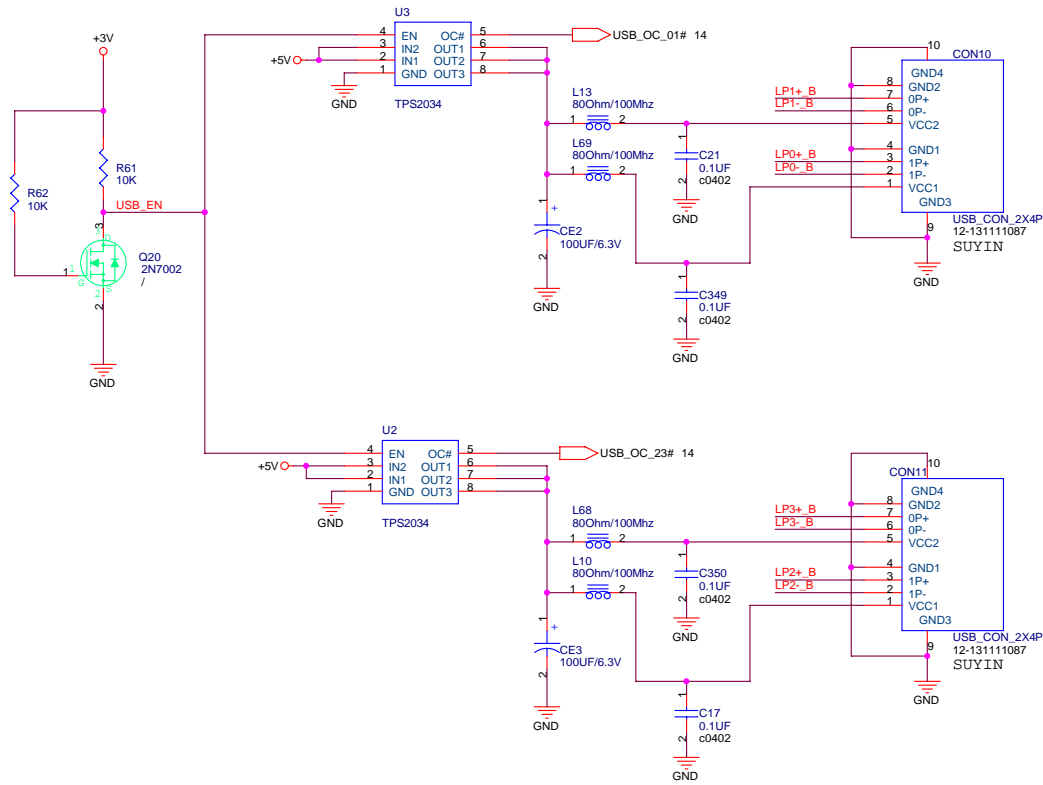
- IDE\_SDIAG:** Connected to +5V via resistor R214 and to GND via a 10kOhm resistor.
- IDE\_DIAI:** Connected to +5V via resistor R37 and to GND via a 10kOhm resistor.
- HD\_CSEL:** Connected to +5V via resistor R414 and to GND via a 470kOhm resistor.



## CD-ROM

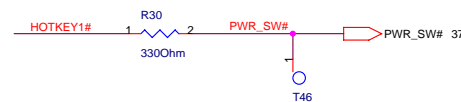
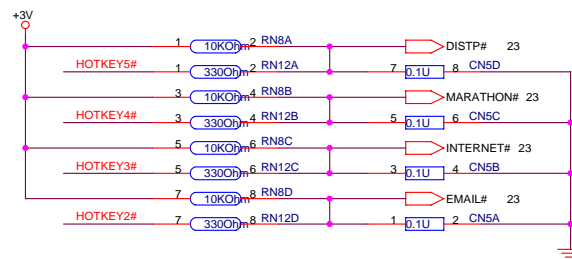
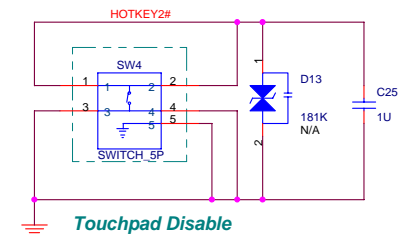
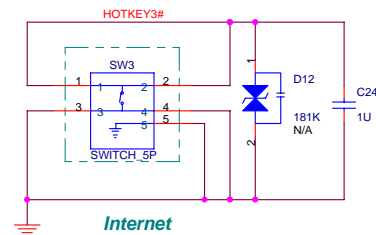
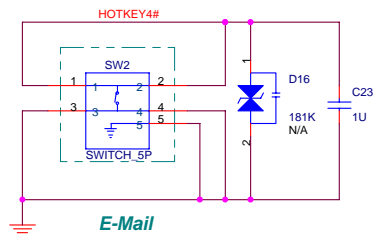
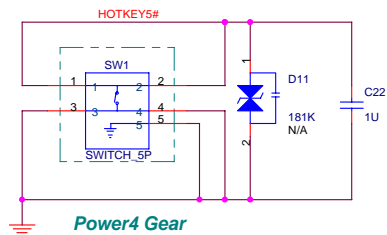


# USB

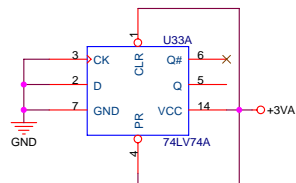
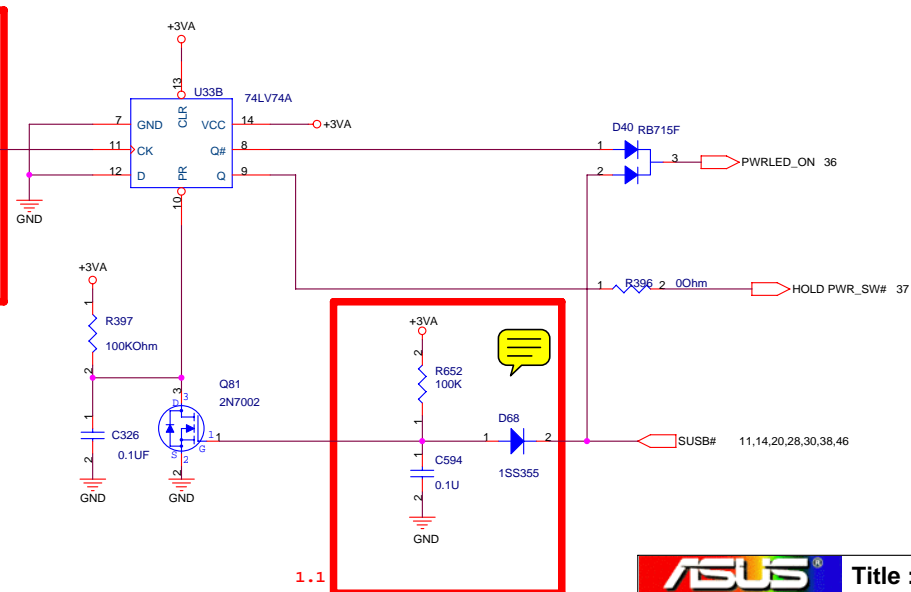
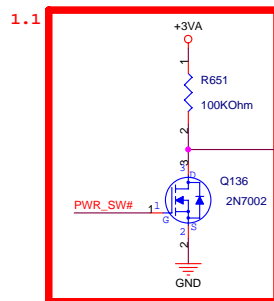


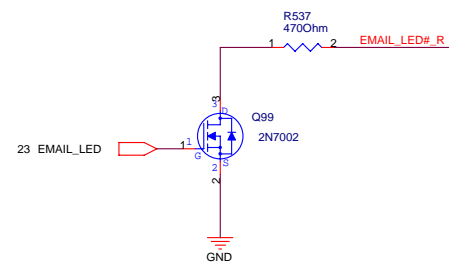
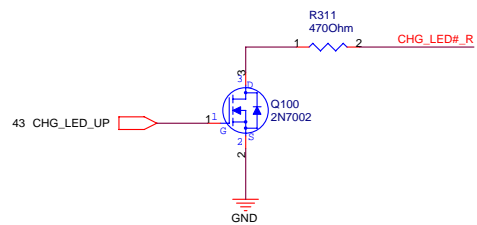
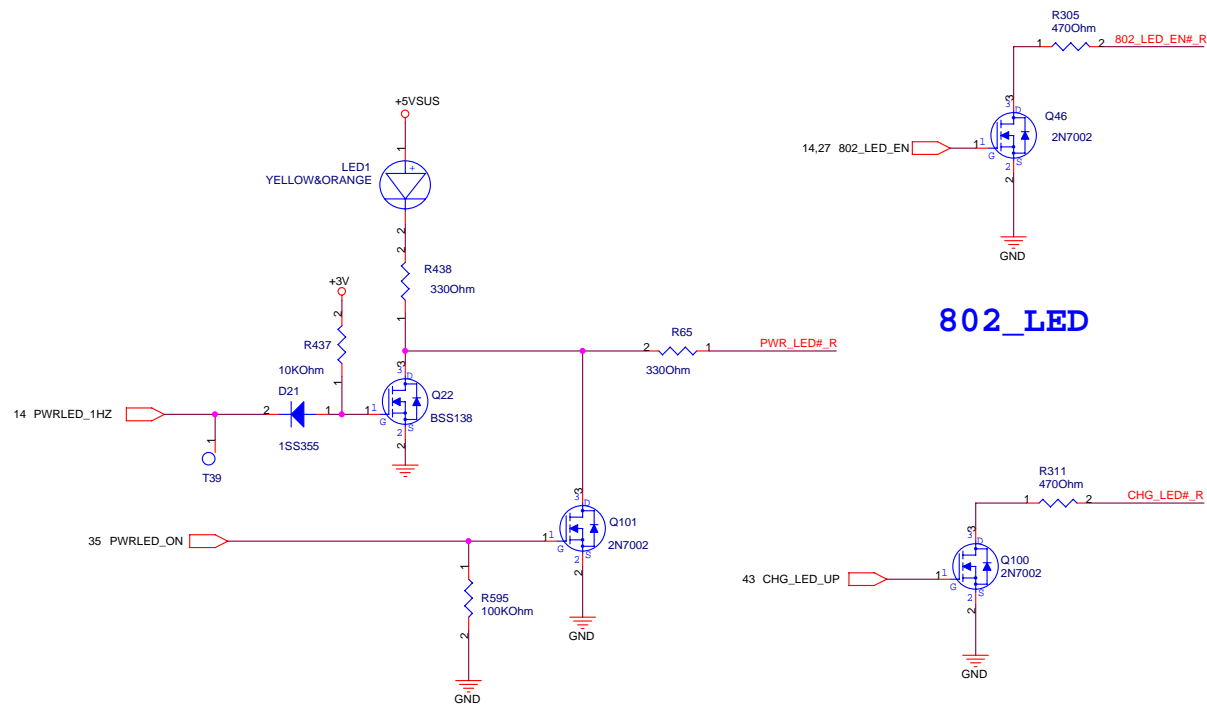
1.1

# FUNCTION KEY

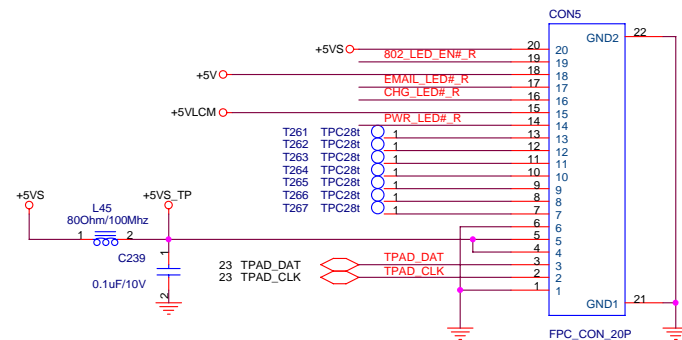
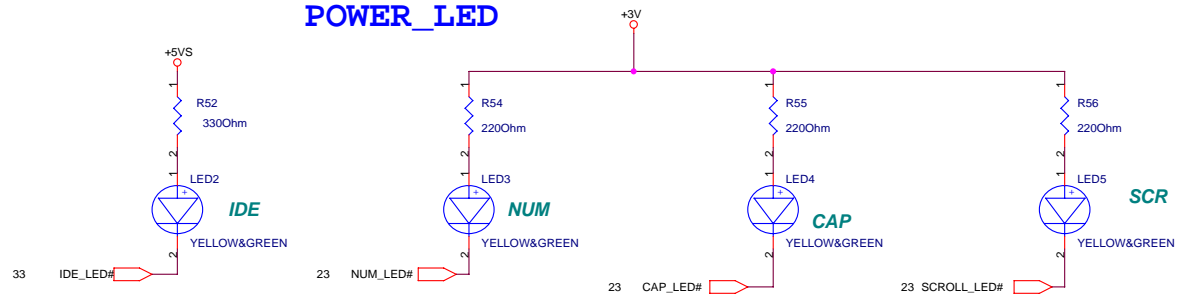


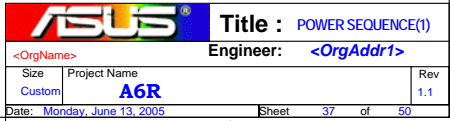
Uses 5-pin switch to improve ESD margin.

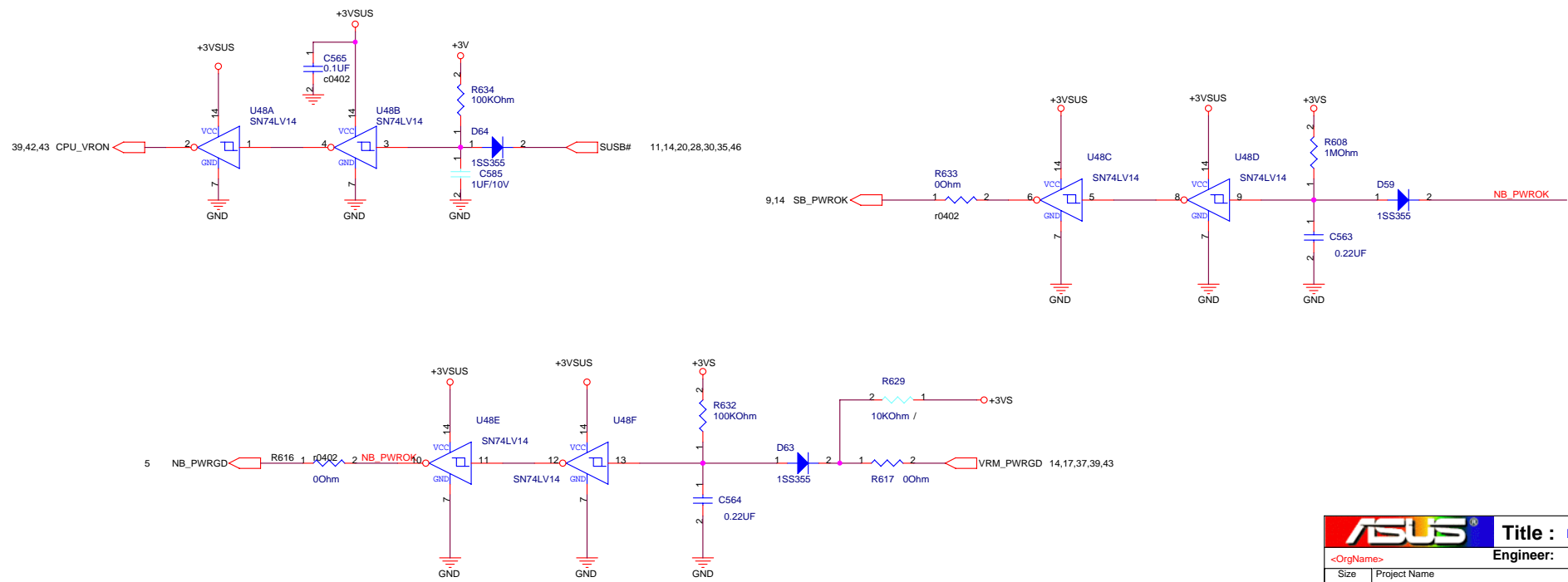
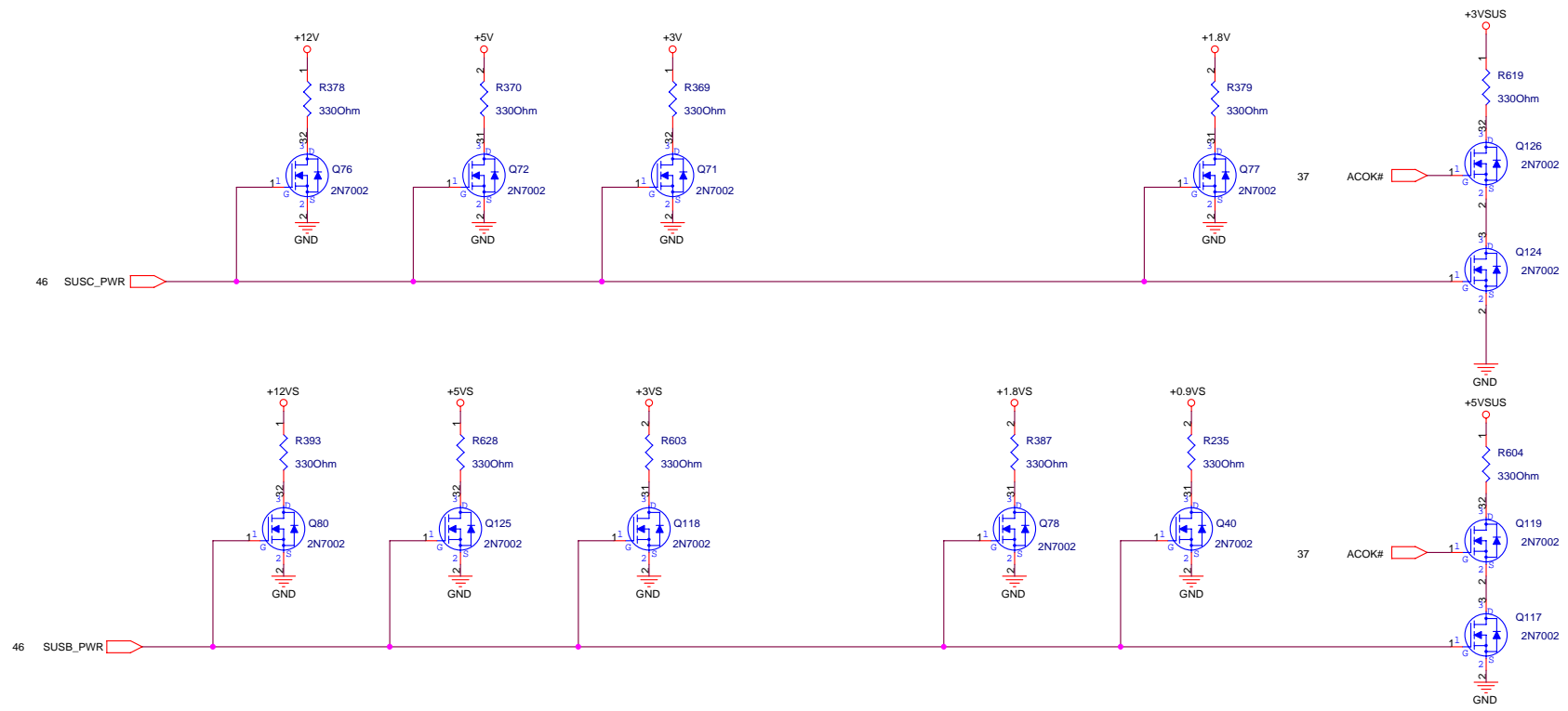


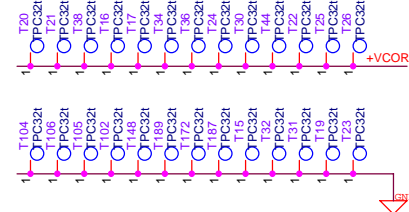
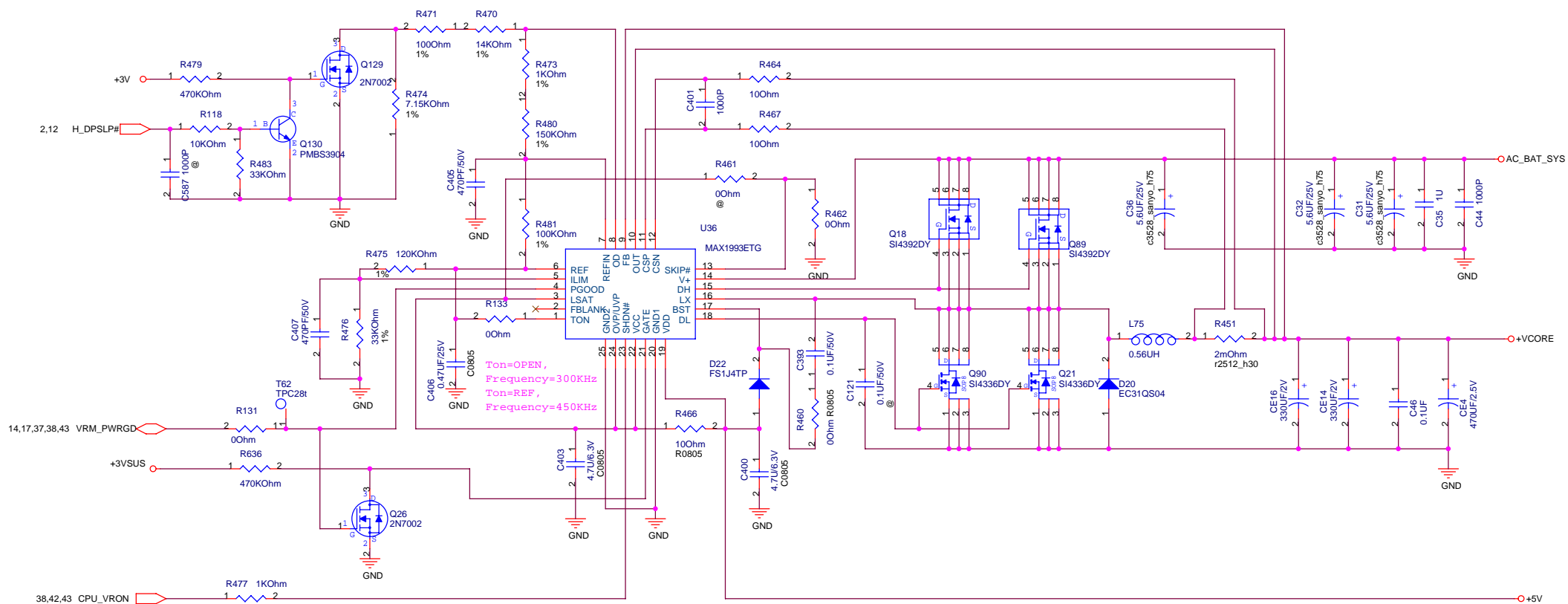


## POWER\_LED





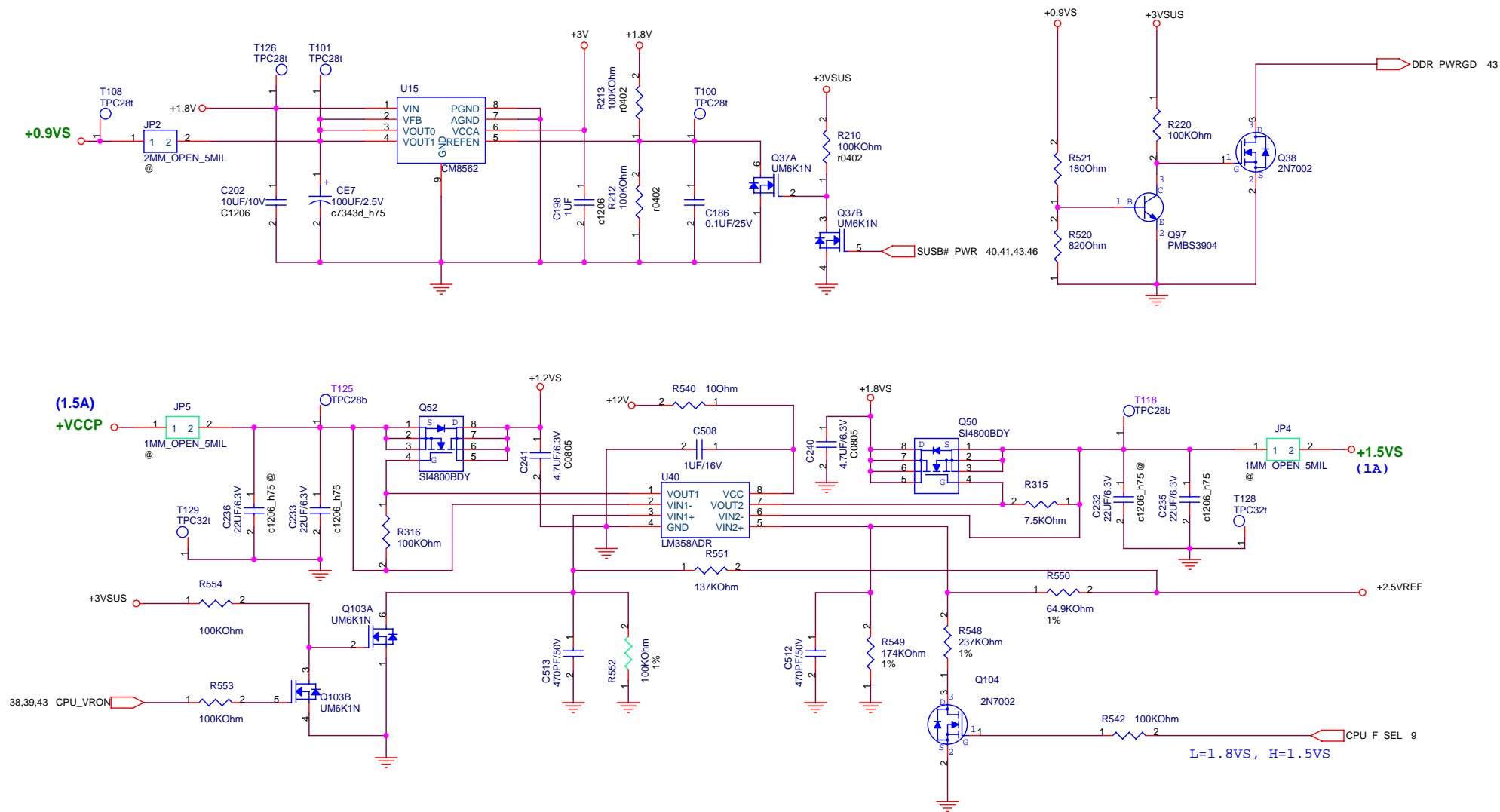


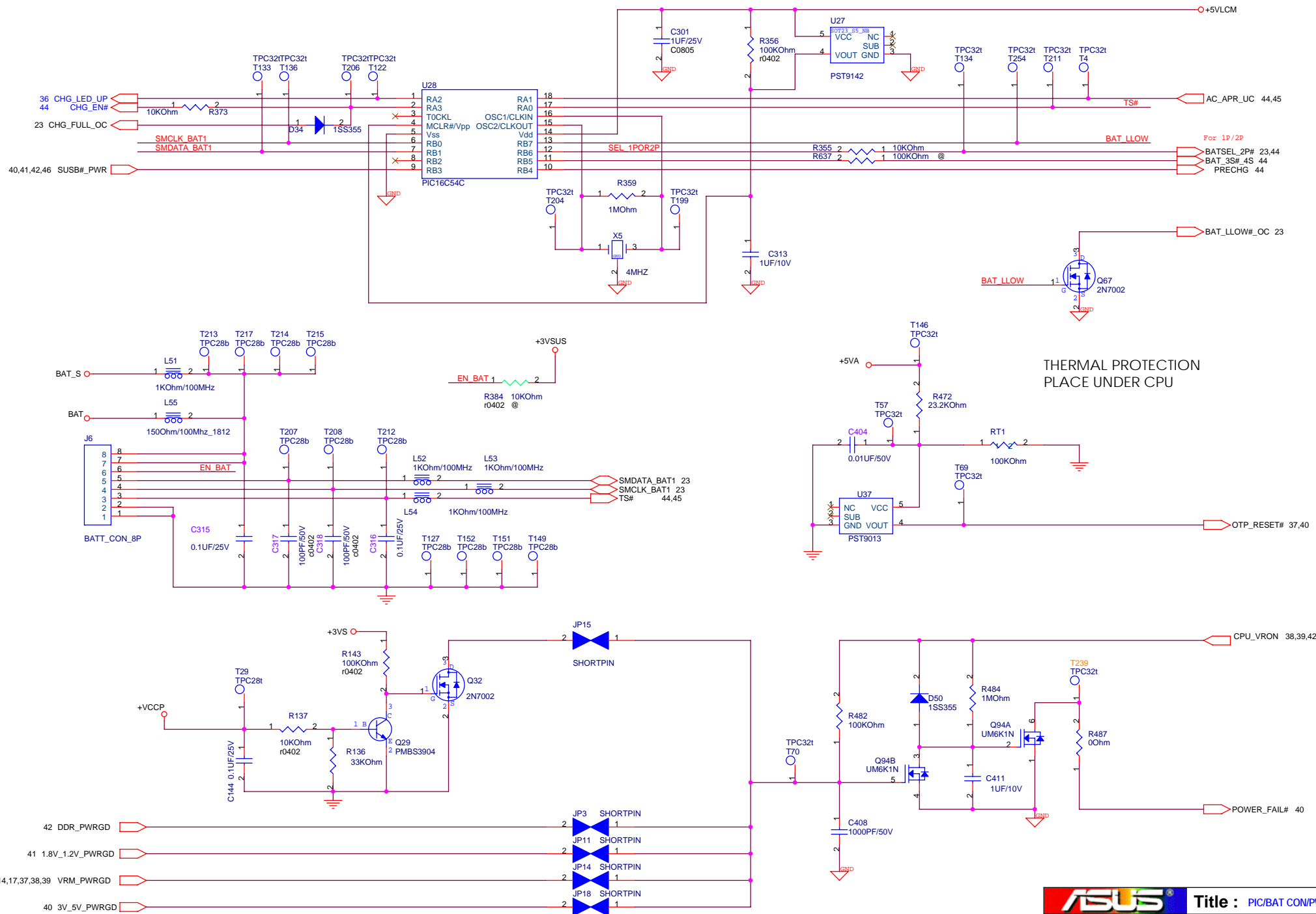






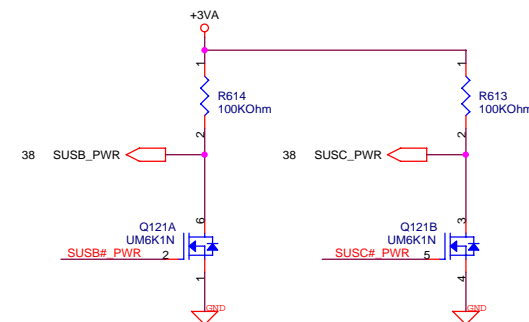
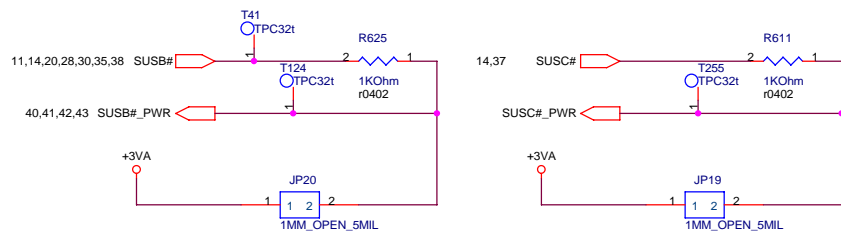
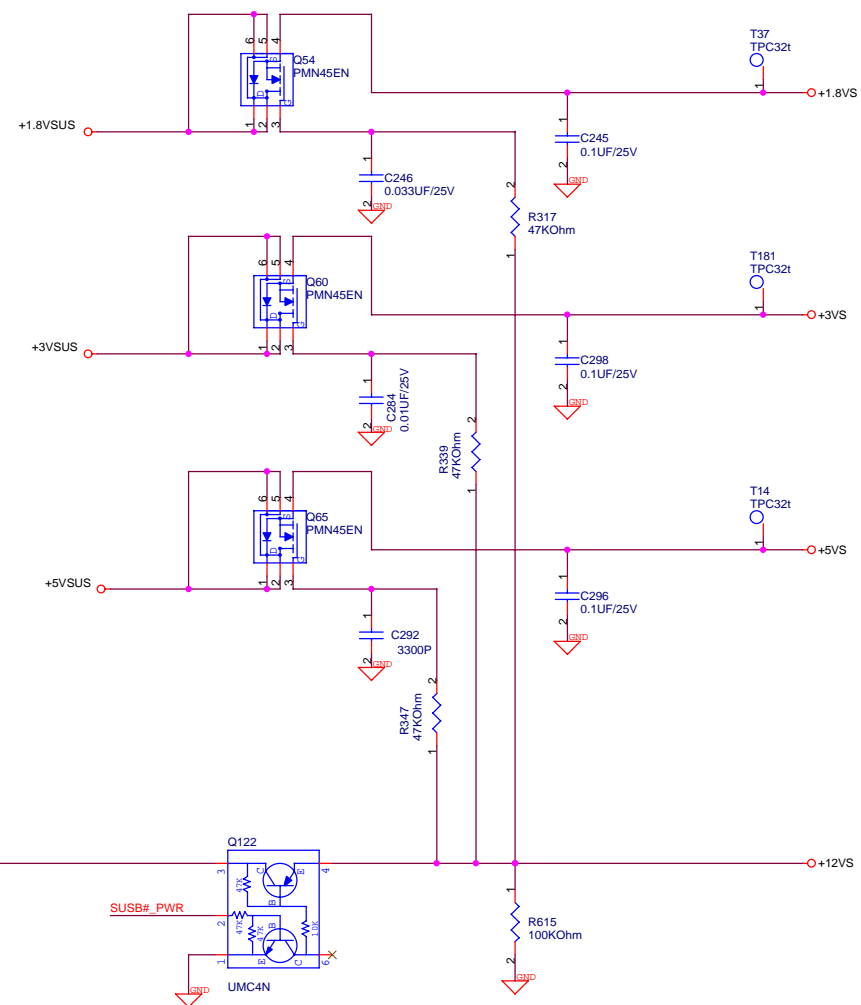
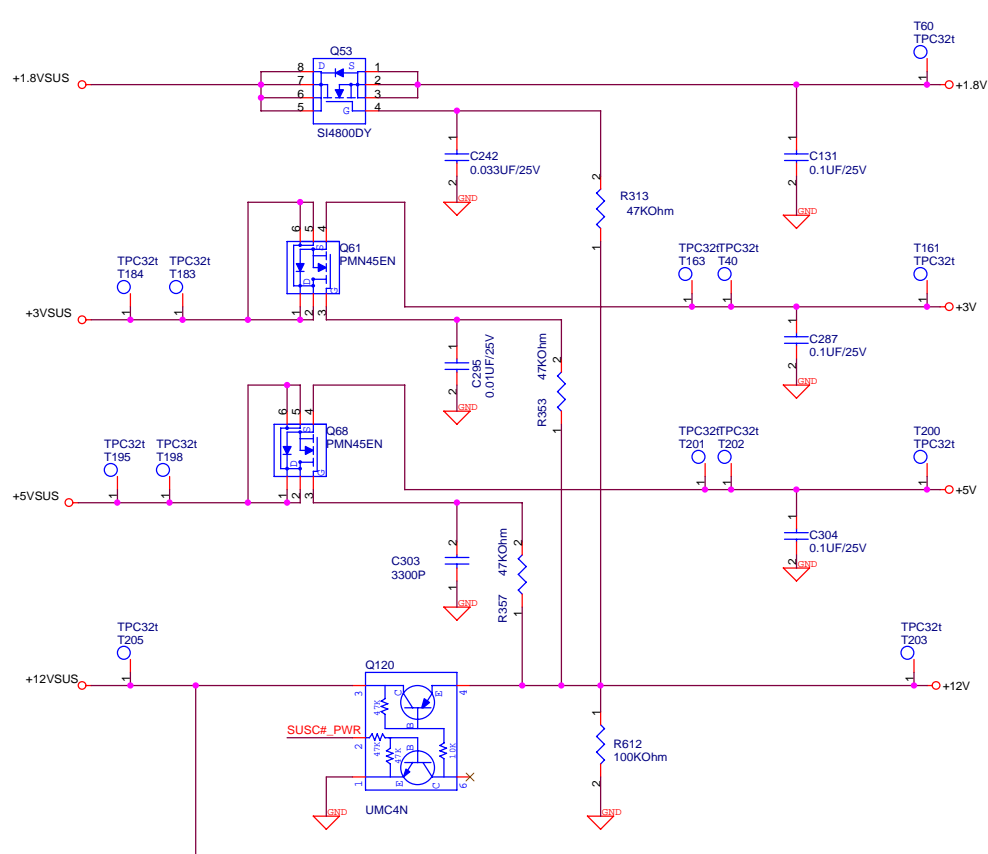


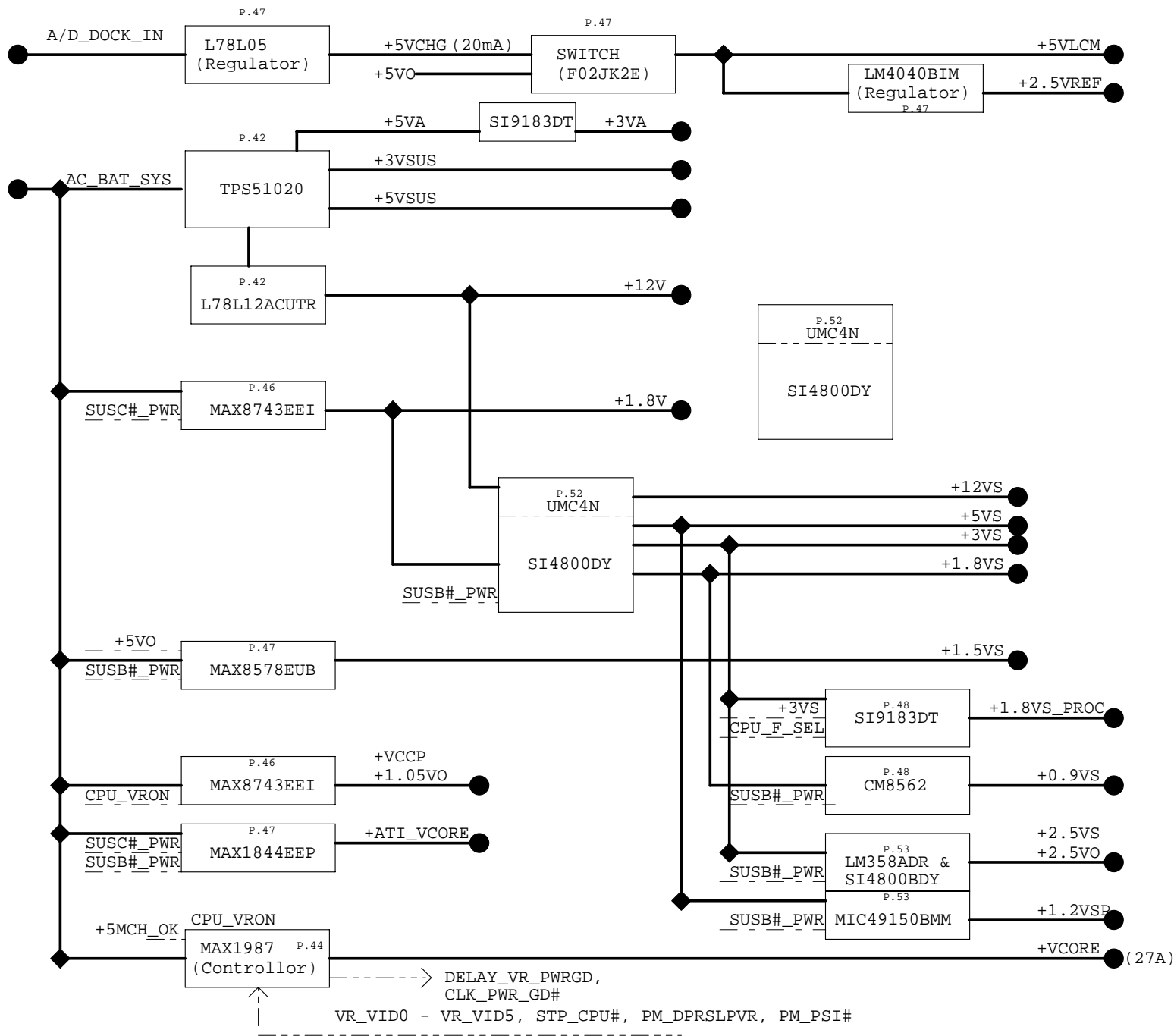












PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI ( 802.11a/b/g )	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor	0101110x ( 5C )
PIC	1001001x ( 92 )

SB400 GPIO TABLE

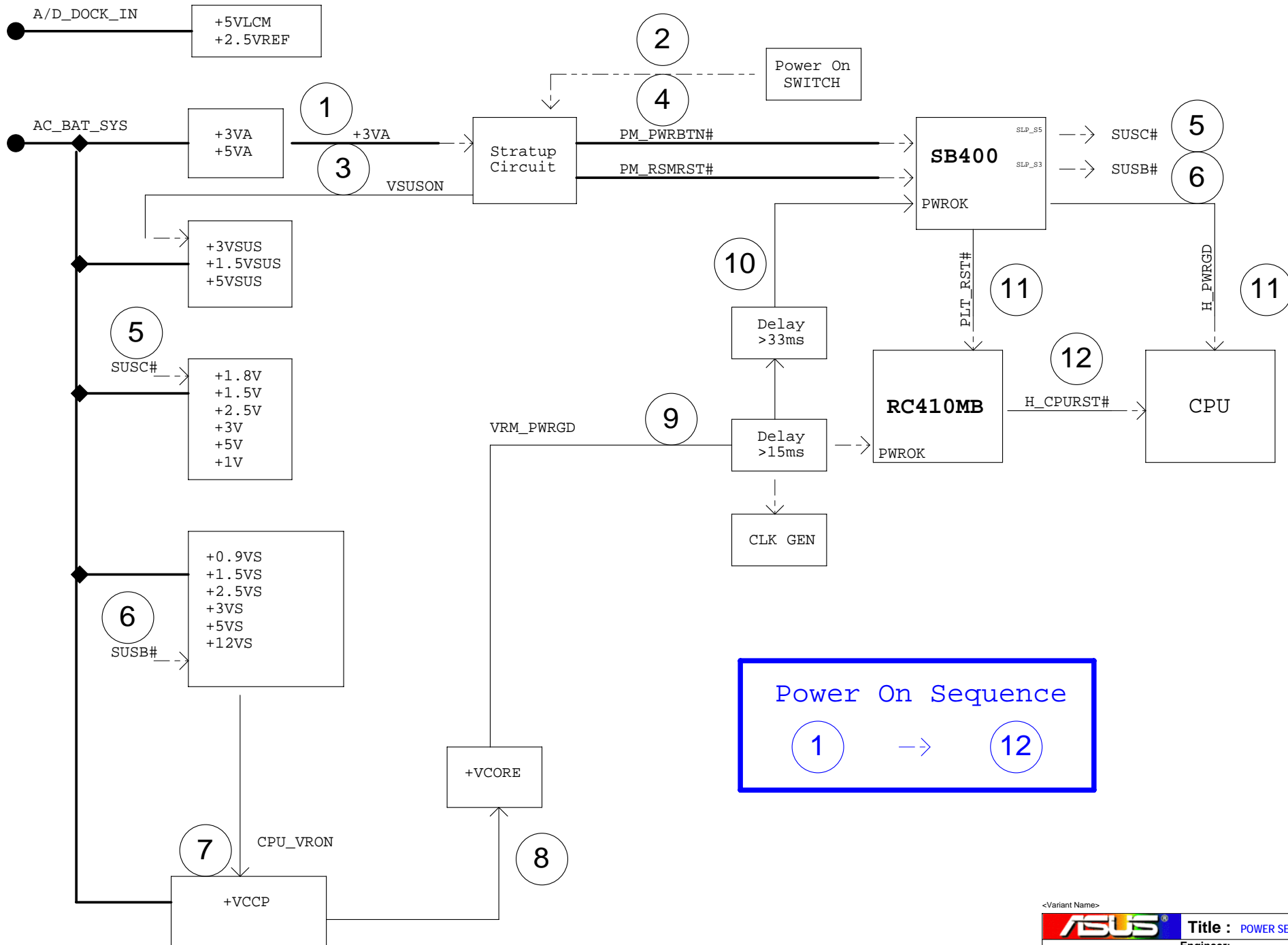
GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	



Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description



Power On Sequence

1 → 12